University “Politehnica” of Bucharest
Faculty of Electronics, Telecommunications and Information Technology

Design of embedded PC (ePC) carrier board for VR HMDs

Dissertation Thesis

submitted *in partial fulfillment* of the requirements for the Degree of Master of Science in the domain *Electronics, Telecommunications and Information Technology*, study program *Advanced Microelectronics*

Thesis Advisor
Ph.D. Corneliu Burileanu

Student
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2018

University "Politehnica" of Bucharest
Faculty of Electronics, Telecommunications and Information Technology
Master program **Advanced Microelectronics (în limba engleză)**

Anexa 2

DISSERTATION THESIS

of student **BADEA Gh. Valentin-Gabriel , 421-AM**

1. Thesis title: Design of embedded PC (ePC) carrier board for VR HMDs

2. The student's original contribution will consist of (not including the documentation part):

• The primary component of the VR HMD shall be the ePC which comprises the SoM core board and carrier board.

• The main activity entails the HW design of the carrier board PCB VR HMD which will be interfaced with the application processor's System-on-Module (SoM) core board.

• Both the size and shape of the PCB needs to be adapted to the mechanical dimensions of the VR HMD enclosure to ensure a compact design. In addition, it is vital to design the carrier board for manufacturability and testability. As such, the BOM list is generated such that the main components of the PCB along with its alternatives are documented. Gerber and drill information files are then generated so that the PCB can be fabricated. Proper practices for EMC should be applied in the design of the schematics and PCB to ensure that the EM emission and immunity complies with the necessary IEC standards for medical devices.

The carrier board shall provide, but the thesis will not discuss all, the following interfaces to the peripherals of the VR HMD.

• HDMI – AV output to the AMOLED/TFT LCD displays and headphones.
• SDIO – SD card for additional storage capacity.
• Bluetooth – Connectivity to user handheld controller.
• USB client – Disk image upgrade, debugging and near IR cameras.
• USB host – Interfacing of additional external peripherals.
• GPIOs – Pushbuttons, LEDs, gyroscope, accelerometer, LiOn battery charge/sense gauge and future expansion.

3. Pre-existent materials and resources used for the project's development:
simulation & CAD software

4. The project is based on knowledge mainly from the following 3-4 courses:
Analog Blocks, Advanced digital systems design, Microcontrollers and Embedded systems

5. The Intellectual Property upon the project belongs to: the company

6. Thesis registration date: 2017-12-05 21:20:34

Thesis advisor(s),
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Student,

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Master program director,
Prof. dr. ing. Claudius DAN

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Validation code: **e544fc6f21**

Statement of Academic Honesty

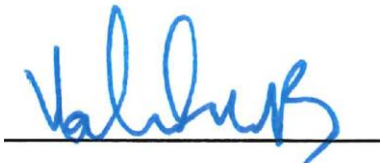
I hereby declare that the thesis „*Design of embedded PC (ePC) carrier board for VR HMDs"*, submitted to the Faculty of Electronics, Telecommunications and Information Technology in partial fulfillment of the requirements for the degree of Master of Science in the domain *Electronics, Telecommunications and Information Technology, study program Advanced Microelectronics*, is written by myself and was never before submitted to any other faculty or higher learning institution in Romania or any other country.

I declare that all information sources sources I used, including the ones I found on the Internet, are properly cited in the thesis as bibliographical references. Text fragments cited "as is" or translated from other languages are written between quotes and are referenced to the source. Reformulation using different words of a certain text is also properly referenced. I understand plagiarism constitutes an offence punishable by law.

I declare that all the results I present as coming from simulations or measurements I performed, together with the procedures used to obtain them, are real and indeed come from the respective simulations or measurements. I understand that data faking is an offence punishable according to the University regulations.

Bucharest, *20.06.2018*

Valentin Gabriel BADEA



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List of Abbreviation

BT	-	Bluetooth®
CAD	-	Computer-aided Design
CPU	-	Central Processing unit
EMI	-	Electromagnetic Interference
ESD	-	Electrostatic Discharge
GPU	-	Graphical Processing unit
HDMI	-	High Definition Multimedia Interface
HMD	-	Head Mounted Device
I2C	-	Inter-Integrated Circuit
IC	-	Integrated Circuit
OS	-	Operating System
PMIC	-	Power Management Integrated Circuit
SD Card	-	Secure Digital Memory Card
SDIO	-	Secure Digital Input and Output interface
SDMMC	-	Secure Digital Multi Media Card
SoC	-	System-on-Chip
SoM	-	System-on-Module
Type-C	-	USB Type-C interface
USB	-	Universal Serial Bus
VR	-	Virtual Reality

Introduction

The VR world began to develop from 1930 and since then a lot of various fields started to implement VRs to ease their tasks or to engage the user deeply into their world. A VR goggle is basically a little screen that makes you feel like you are a part of the viewed content. You can interact on some level with that world and you will be impressed by how accurate things can look in VR. Although, the main reason of this application is for entertaining, the technology can be used also for much more important applications like learning process or medical treatments. In this thesis the main scope of the VR goggle developed is for the medical usage. Here, a deep experience can treat patients with different psychologic problems like phobia. Therefore, to design these VR goggles some requirements were defined for entire product envision and development:

- Price (cheap, has to be available to many users in many pathologies)
- Form-factor (as small and compact as possible to not impair the user movement)
- Performance (to be able to run content for at least 2 years after the market release)
- Reliable (doctors and patients should trust the abilities of this product that is reliable to be used safely in the clinical environment)

Fig. 0.1 Samsung VR Gear

To begin with, the system needs to have a processing power whose performance can fulfill the VR content (heavily graphical) requirements. Nowadays, the SoCs embedded a powerful GPU that can satisfy the VR applications. The first criteria to choose a proper SoC is the type of OS that will run on it and the ease of content development. When it comes to OS there is one with a big community support, open source and with high compatibility between different drivers, that is, Android. The main advantage of Android is that it already has a homogenous environment for developing for all branches of technology that this project has interest in. The time for software and content development in this OS architecture, documentation and support availability for drivers from many peripherals manufacturers and also the performance, made Android's cost-time-performance ratio to be competitive and decisive in winning the software platform for the product.

To preserve and augment Android's platform advantages, a proper hardware platform need to be choose. The key characteristics are price and performance. For the first prototype, flexibility is also considered. The Rockchip 3399 CPU fits well with all requirements and it is available in the form of a SoM which reduces the development time of the final hardware part. A SoM is a SoC which has additionally the volatile and non-volatile memories on the same module. For the current SoM, a carrier board must be designed to create the SoC interfaces.

I. Carrier Board Design

The VR goggle needs to have:

- WIFI/ BT connectivity
- 2x USB 2.0 ports
- USB Type-C 3.1 with Power Delivery
- HDMI output
- microSD card slot (SDR104)
- Accelerometer & Gyroscope
- 1.5h runtime

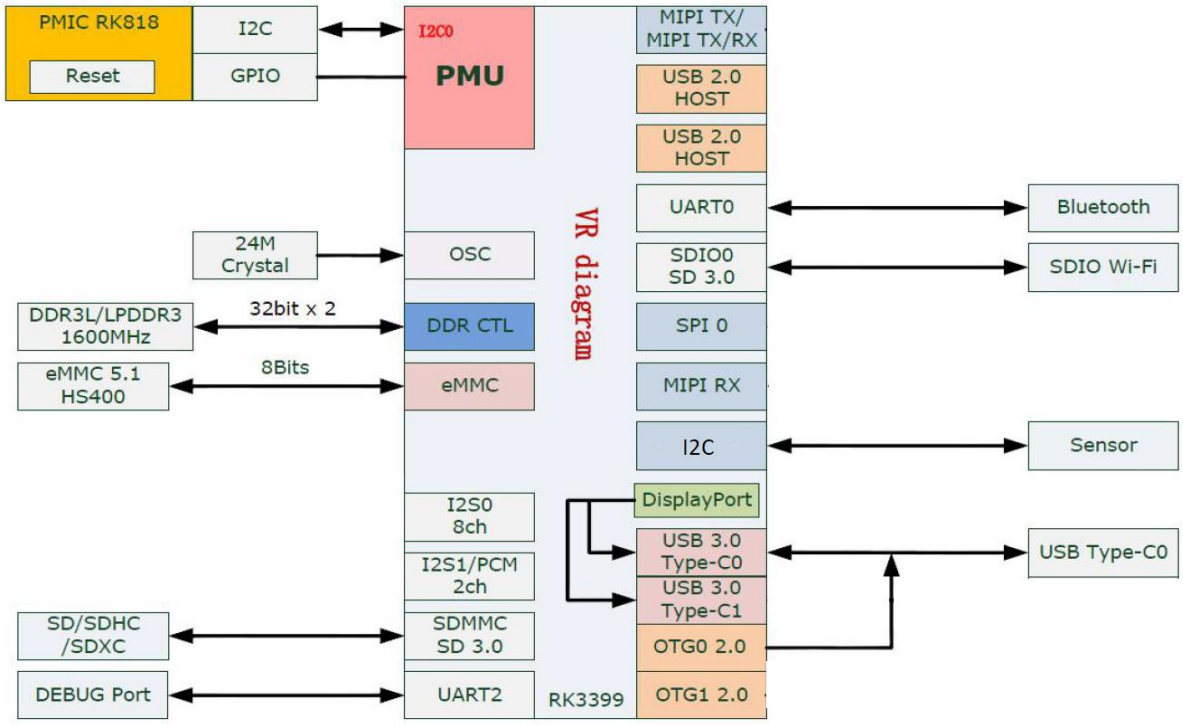


Fig. I.1 Block diagram of the system

Keeping in mind the main requirements of this product, all the following device choices and their reasoning are described in this thesis. For all design purposes was used Altium 18.1, which turned out to be a suitable CAD environment for a complex PCB project like this.

1. High Speed Interfaces

1.1. USB

The Universal Serial Bus is a common way for attaching keyboards, mice, printers, microphones and lots of other kinds of devices to desktop and laptop computers. This connector supplies both power and data to peripherals. It will be used in the presented product as an input line for keyboard and mouse. There are currently 3 main standards of USBs that are currently available on the market, version 2.0, 3.0 and newly launched USB 3.1.

USB 2.0 was released in April 2000, adding a higher maximum signaling rate of 480 Mbit/s (High Speed), in addition to the USB 1.x Full Speed signaling rate of 12 Mbit/s. Due to bus access constraints, the effective throughput of the High Speed signaling rate is limited to 280 Mbit/s or 35 MB/s [1]. This standard will be used for keyboard and mouse because it is wide spread through all devices.

The USB 3.0 specification was released on 12 November 2008 and adds a SuperSpeed transfer mode, with associated backward compatible plugs, receptacles and cables. SuperSpeed plugs and receptacles are identified with a distinct logo and blue inserts in standard format receptacles.

The USB connectors are widely available in many forms. The most common USB used for the keyboards and mice is the USB 2.0 Type-A.

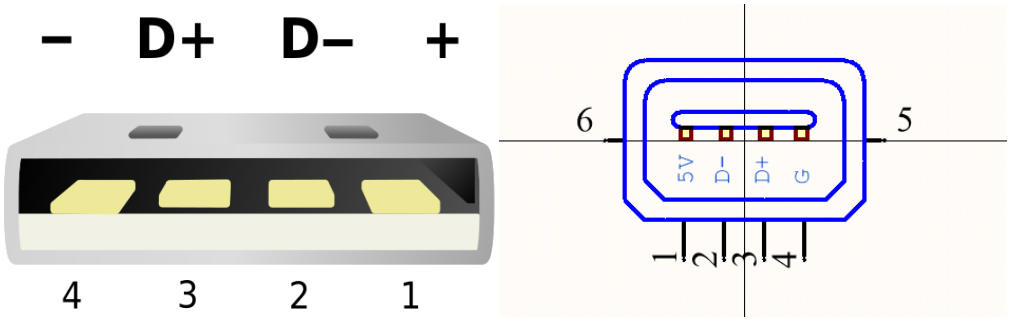


Fig. I.2 USB-A pinouts and schematic symbol

Connector has 4 pins: VCC, D-, D+ and GND. Also, is recommended to connect the casing to a solid GND connection to improve signal shielding (pins 6 and 5 from schematic symbol); VCC must be connected to a 5V source to provide power to the peripheral connected. The D-/D+ are differential data pairs and GND connects to the system ground. Figure 3 shows the schematic of the USB connector.

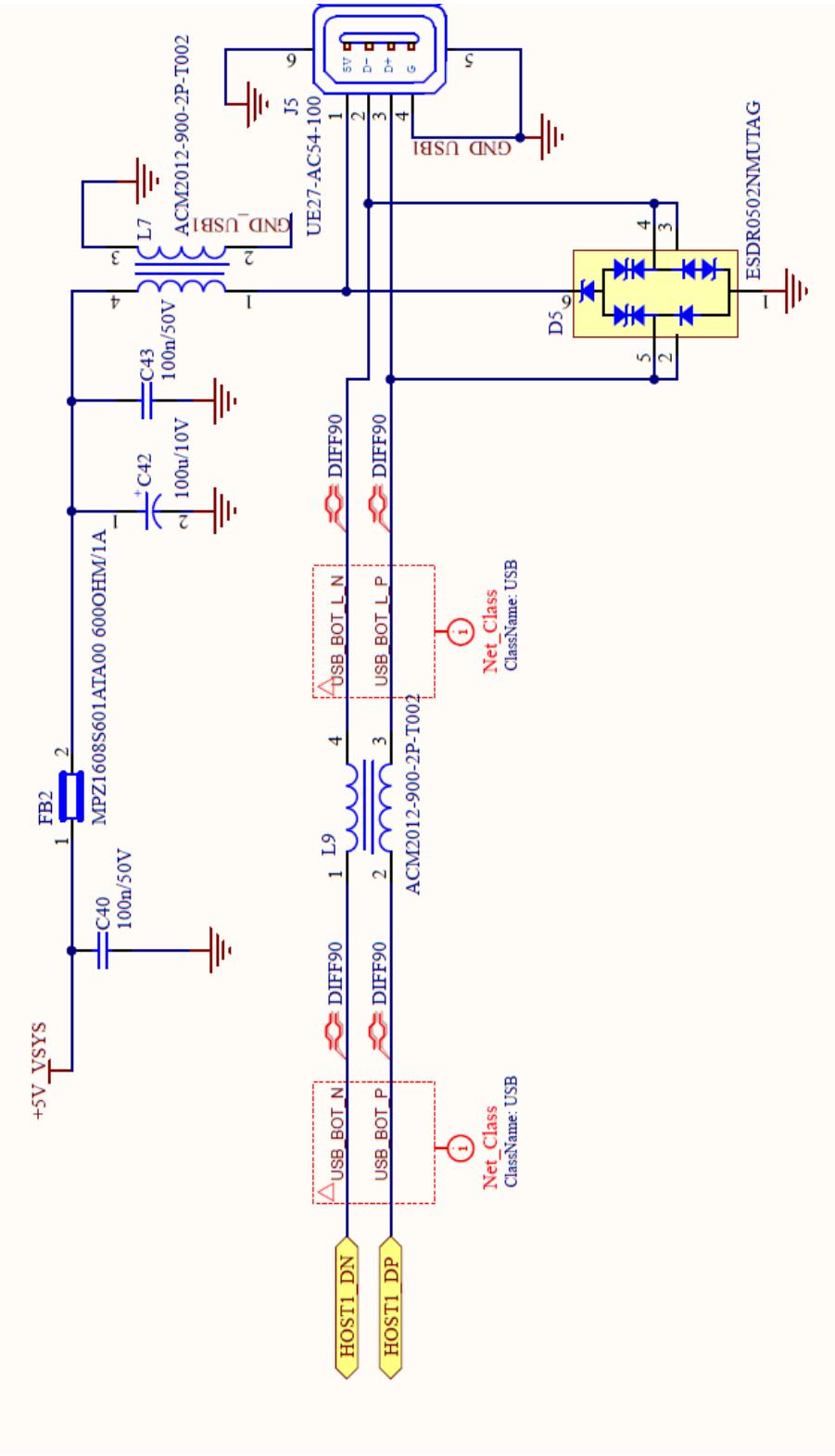


Fig. I.3USB-A schematic

1.2. USB 3.1 Type-C

The latest major improvement in the USB standard is the speed. The new USB 3.1 adds the new transfer rate referred to as SuperSpeed USB (SS) that can transfer data at up to 10 Gbit/s. Manufacturers are recommended to distinguish USB 3.1 connectors from their USB 2.0 counterparts by blue color-coding of the Standard-A receptacles and plugs, and by the initials SS. The USB 3.1 speeds are incorporated in the new Type-C connector, which, beside the improved transfer rate, can provide a larger power to the system through the new USB PD 1.2 standard.

USB Type-C port and cable layouts are shown in figure 4. Flipping the plug does not cause any problems due to the symmetrical design of the signals in the receptacle port. The USB 3.1 SuperSpeed TX/RX, VBUS, GND and other pins are connected correctly regardless of the orientation of the plug and receptacle. From a user standpoint, this approach is an upgrade from Type-A ports, as the Type-C cable can be inserted in either direction. USB Type-C is versatile and user-friendly, but this ease of use increases the internal complexity for devices that employ the technology. It has increased power capability, but that creates issues for devices that do not require so much power. This is where the PD protocol is useful. PD ensures that the appropriate range of power is delivered or sourced from any connected devices. The Type-C for this application provides the power to charge the battery and also to power the system by its own because it can deliver 3A at 5V which means a power of 15W.

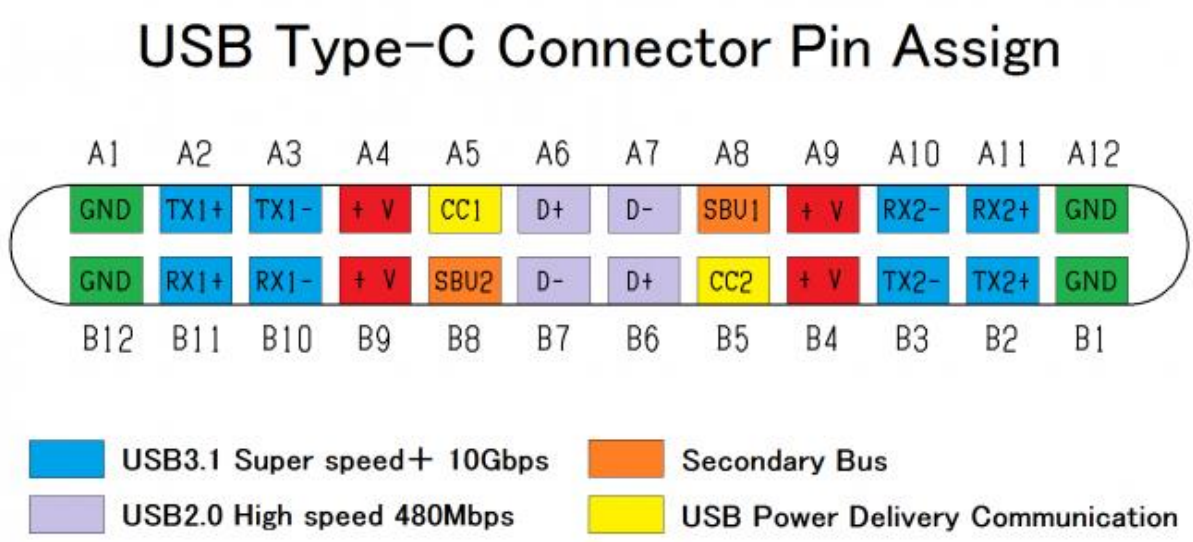


Fig. I.4 Type-C connector pin-out

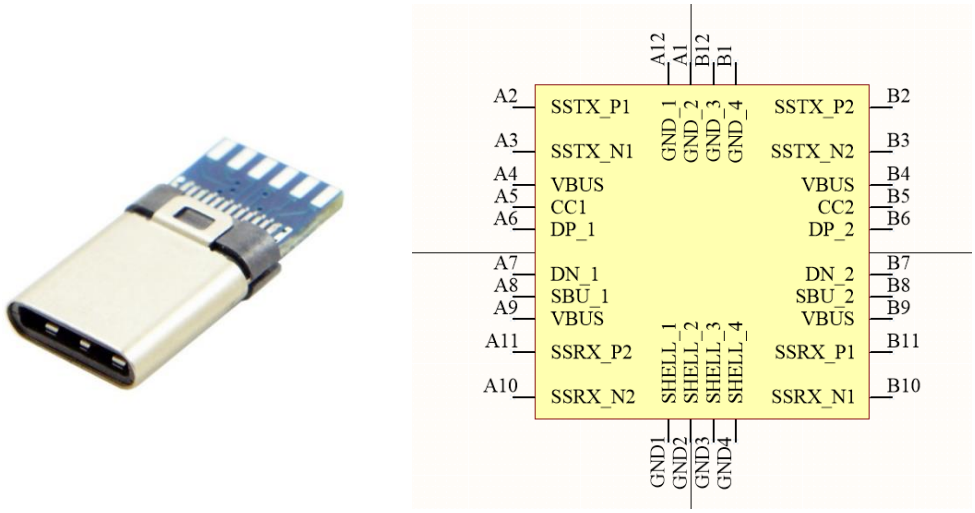


Fig. I.5 Type-C connector

Before discussing USB Type-C, it's important to distinguish between the device, the host, the power supplier (source) and the power receiver (sink). The host is not always the source; therefore, the terms ca not be used interchangeably. Hosts initiate all the communication and devices respond. Typically, the host is the downstream-facing port (DFP) and the device is the upstream-facing port (UFP). If two hosts are connected, they can act as a dual-role port (DRP) to switch between acting as a host and a device. For example, when a keyboard is connected to a laptop, the keyboard is the UFP and sink, while the laptop is the DFP and source [2].

The initial power-delivery agreement between connected devices is executed through a series of resistors acting as voltage dividers on CC wires when a Type-C plug is inserted into the receptacle. Figure 6 shows a typical USB Type-C channel line topology.

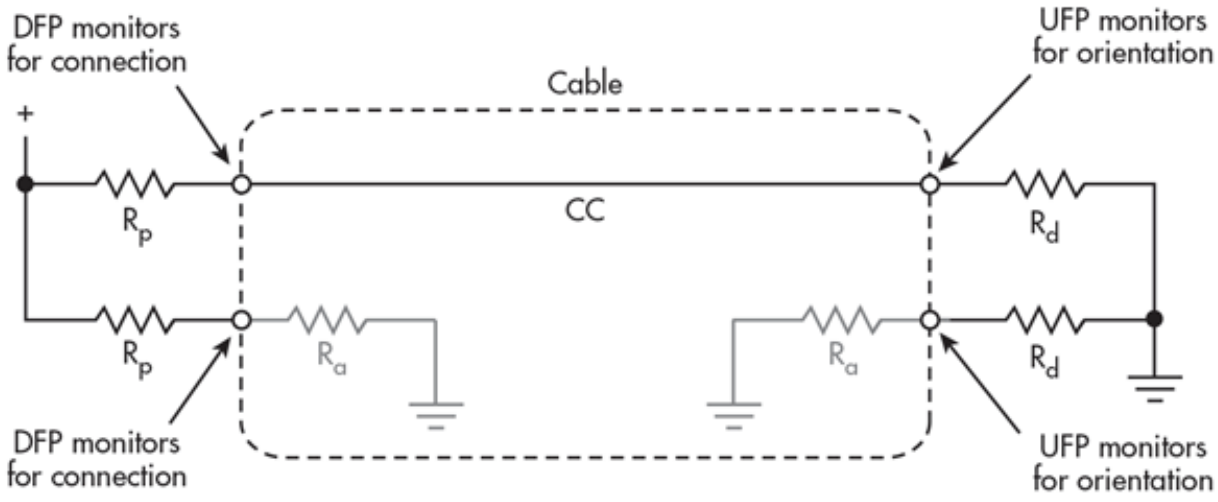


Fig. I.6 USB Topology

Since the CC line in the plug is either connected to CC1 or CC2 in the receptacle, the receptacle determines the orientation of the plug by simply measuring the voltages on both CC1 and CC2 lines. The different values of the pull-up resistors communicate the amount of current the source can supply and establishes what will be the UFP and the DFP. The power consumer does not have a way to indicate how much current it sinks through different pull-down resistor values; it must dynamically adapt its load to match the maximum current available from the provider.

To read the voltage divider correctly, both devices need an analog processing unit, usually in the form of an accurate analog-to-digital converter (ADC) within an MCU. The ADC measures the voltage on the CC line continuously to monitor the connection between the plug and the receptacle. The MCU, known as the PD controller, in this case, FUSB302 which handles the complete physical layer and upper layer protocol. It negotiates the power being delivered or received. For simple Type-C applications, the power negotiation stops with the resistors. For a more adaptable design, though, the devices can agree on a different setup by communicating over the CC line. Once the plug orientation and initial power are decided, the devices use the CC line to communicate with each other. Using this line, the devices can agree on different levels of power and designate the sink or source, enabling real-time power-delivery adaptation. CC line communication is also used to announce which type of communication will be used. As previously stated, USB Type-C can communicate on the high-speed lines, USB 2.0, and other lines. The devices announce which of these lines can be used via the CC line. However, not all devices support all communication protocols. Because the CPU does not support this function, a separate IC was introduced to manage communications on the CC line and send the information to the CPU.

The FUSB302 enables the USB Type-C detection including orientation. Also, integrates the physical layer described previously for PD protocol and communicates with the CPU through I2C bus.

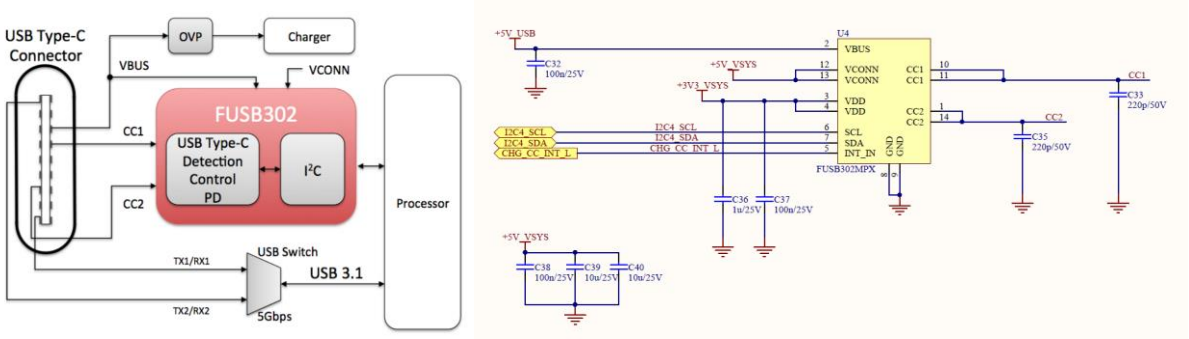


Fig. I.7 USB Type-C detection circuit

Being a connector available outside the casing, it must be protected with ESD. Same ESD device is used as in SD card situation. Also, common mode filters need to be placed on lines. It was used the same series as for the USB 2.0 but with a higher cutoff frequency due to high speed signals of USB 3.1.

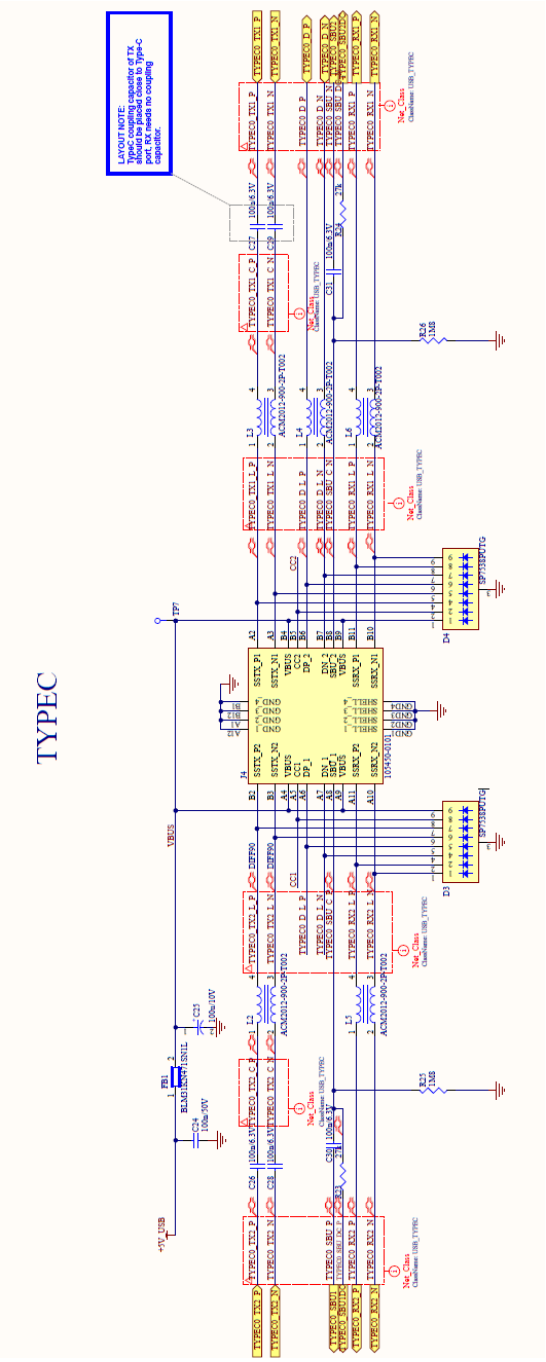


Fig. I.8 USB Type-C Schematic

1.3. HDMI

HDMI technology is the industry-leading interface and de-facto standard connecting high-definition (HD) and ultra-high-definition (UHD) equipment, from HDTVs and personal computers to cameras, camcorders, tablets, Blu-ray players, gaming consoles, smartphones and just about any other device capable of sending or receiving an HD signal. By delivering crystal-clear, all-digital audio and video via a single cable, HDMI technology dramatically simplifies cabling and helps provide consumers with the highest-quality HD experience. It supports 8-channel, 192kHz, uncompressed digital audio and all currently-available compressed formats, with bandwidth to spare, can accommodate future enhancements and requirements. The current project uses HDMI 2.0 to output video and audio signal through a projection device. Without this interface the user can no see his interaction with the system.

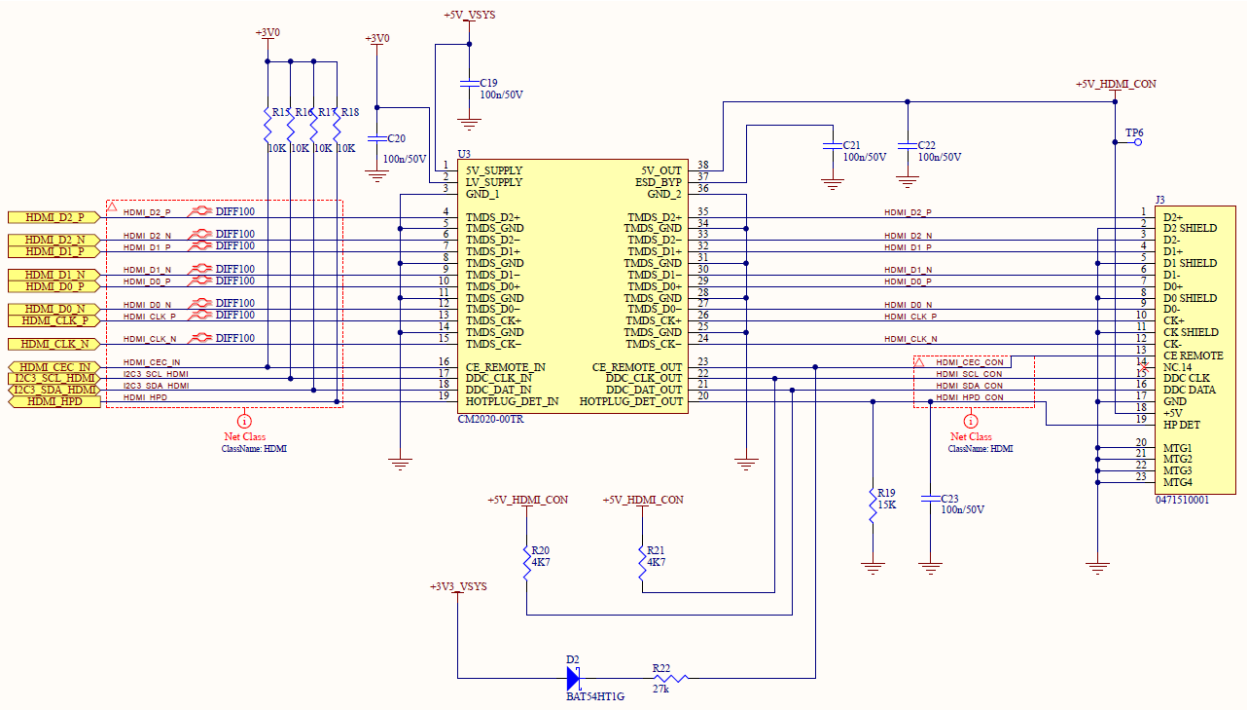


Fig. I.9 HDMI Schematic

HDMI has three physically separate communication channels, which are the DDC, TMDS and the optional CEC.

The Display Data Channel (DDC) is a communication channel based on the I²C bus specification. HDMI specifically requires the device implement the Enhanced Display Data Channel which is used by the HDMI source device to read the E-EDID data from the HDMI sink device to learn what audio/video formats it can take. HDMI requires that the E-DDC implement I²C standard mode speed (100 Kbit/s) and allows it to optionally implement fast mode speed (400 Kbit/s).

Transition-minimized differential signaling (TMDS) on HDMI interleaves video, audio and auxiliary data using three different packet types, called the Video Data Period, the Data Island Period and the Control Period. During the Video Data Period, the pixels of an active video line are transmitted. During the Data Island period (which occurs during the horizontal and vertical blanking intervals), audio and auxiliary data are transmitted within a series of packets. The Control Period occurs between Video and Data Island periods.

Consumer Electronics Control (CEC) is an HDMI feature designed to allow the user to command and control up to 15 CEC-enabled devices, that are connected through HDMI, by using only one of their remote controls [3]. The system uses the regular connector although it could be used a smaller version of it (mini HDMI or micro HDMI). The bigger version is preferred because this is the most widely used HDMI connector and the space on the board was enough to fit it. If the dimension of the PCB comes into discussion and needs to be shrunken, this is one part that can be replaced with a smaller version.

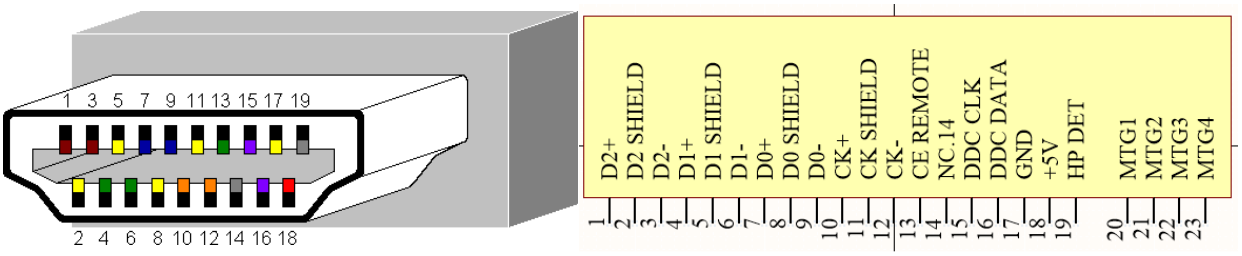


Fig. I.10 HDMI Connector and Symbol

HDMI needs also protection against ESD, overcurrent and back-drive. The CM2020−00TR incorporates all these protections and also level shift, from 3.3V to 5V and overcurrent protection. The EMI protection is not necessary to implement because the quality HDMI cables are shielded, the connector is shielded and having in mind the high speed of the HDMI 2.0 that can go up to 360MHz, another capacitance will degrade de signal integrity on TDMS lines.

1.4. SD Card

The SD card is a non-volatile memory used to extend the system storage space. It comes in 3 different sizes: normal, mini, micro. For this application it's used the micro version. The extra storage can be used as an input interface for software that will run on the VR goggles.

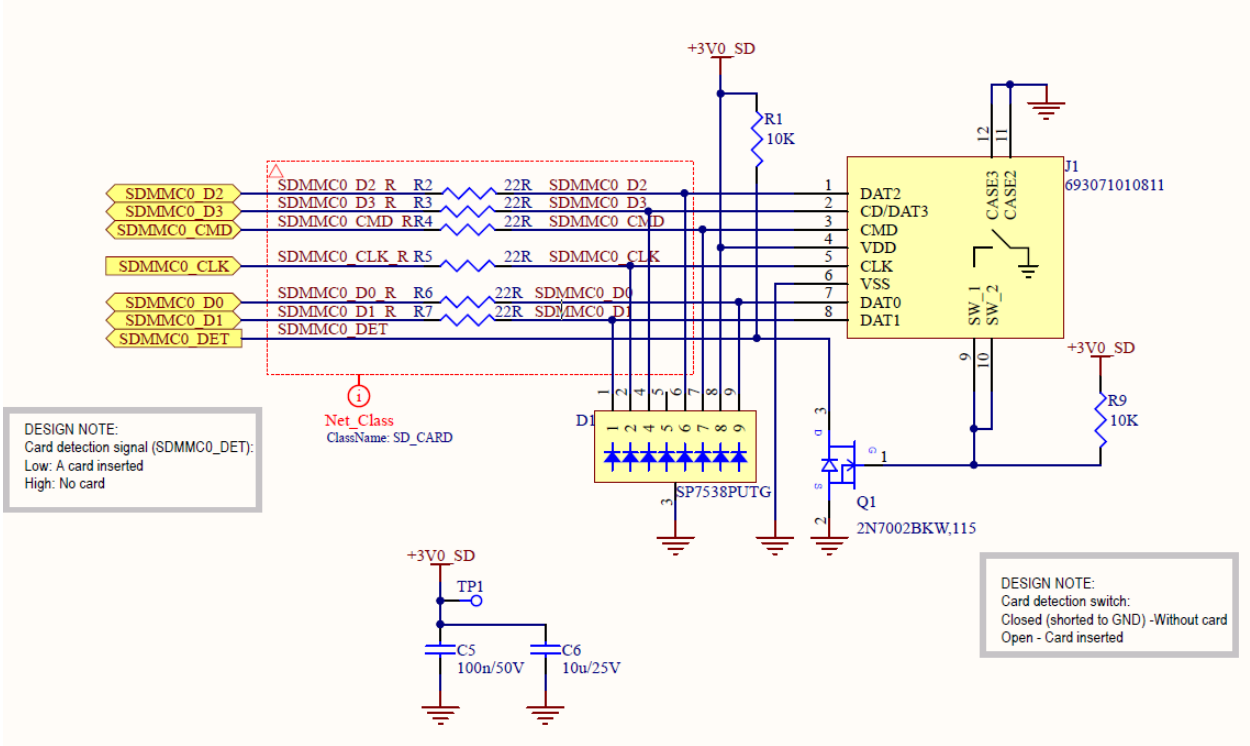


Fig. I.11 SD Card schematic

It communicates through SD/MMC interface. The interface speed depends on the card inserted, but the current system can perform up to 104 MB/s (SDR104). This qualifies for the first category of Ultra-High-Speed standard for SD cards. There are several categories depending on the bus speed described in table 12.

Bus interface	Card logo	Bus logo	Bus speed
Default Speed	SD SDHC SDXC	—	12.5 MB/s
High Speed			25 MB/s
UHS-I	SDHC SDXC	I	12.5 MB/s (SDR12) 25 MB/s (SDR25) 50 MB/s (SDR50, DDR50) 104 MB/s (SDR104)
UHS-II		II	156 MB/s (FD156) 312 MB/s (HD312)
UHS-III		III	312 MB/s (FD312) 624 MB/s (FD624)

Fig. I.12 SD Cards speed ratings

Clock signal frequency for SDR104 is 208MHz. The system can accommodate various types of card due to its ability to change the supply voltage. SD card should always be supplied 3.0V and CPU SD interface default level is 3.0V. When the SD card is inserted, the signal communication level of the interface is based on 3.0V. After negotiation of the communication, if the SD card is a SD3.0, which can support USH-I high speed protocol, CPU will adjust the interface level value to 1.8V through adjusting the PMIC output. There is an LDO and a power switch embedded in the SDMMC interface. The LDO and power switch are controlled automatically by CPU to provide appropriate voltage according to the type of card inserted.

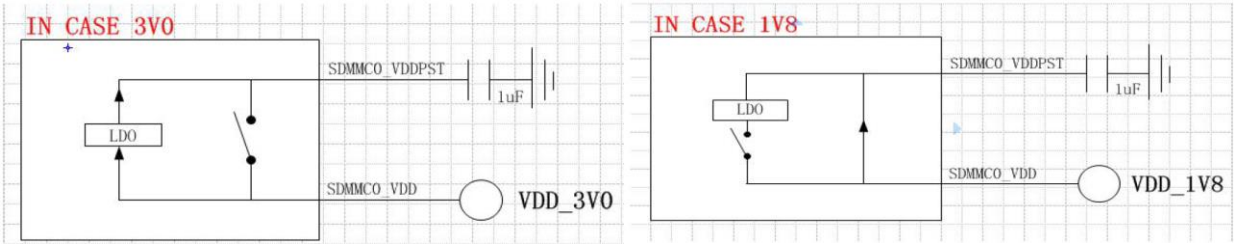


Fig. I.13 SD Card power circuit

To detect if the card is inserted a N-channel MOSFET is used. The connector has a switch which is open when the card is not inserted. This switch and the CPU input pin are pulled-up by default. When the card is inserted into the connector, the switch pulls down the N-channel gate which translates to a low signal on the detection input pin. So, when the card is connected, the level is low, otherwise it is high.

Like other output interfaces, this needs to be protected against ESD. All data lines and power are level 4 protected and the parameter important for the signal integrity, the junction capacitance, is kept low as 0.3 pF. The load capacitor including SD card and PCB, should be less than 10 pF.

1.5.Gyroscope

Inexpensive vibrating structure microelectromechanical systems (MEMS) gyroscopes have become widely available. These are packaged similarly to other integrated circuits and may provide either analog or digital outputs. In many cases, a single part includes gyroscopic sensors for multiple axes. Some parts incorporate multiple gyroscopes and accelerometers (or multiple-axis gyroscopes and accelerometers) to achieve output that has six full degrees of freedom. These units are called inertial measurement units, or IMUs. Internally, MEMS gyroscopes use lithographically constructed versions of tuning forks or vibrating wheels.

Tuning forks

This type of gyroscope contains a pair of test masses driven to oscillate with equal amplitude but in opposite direction. When rotated, the Coriolis force creates an orthogonal vibration that can be sensed by a comb type structure. Their displacement from the plane of oscillation is measured to produce a signal related to the system's rate of rotation. F. W. Meredith registered a patent for such a device in 1942 while working at the Royal Aircraft Establishment [4].

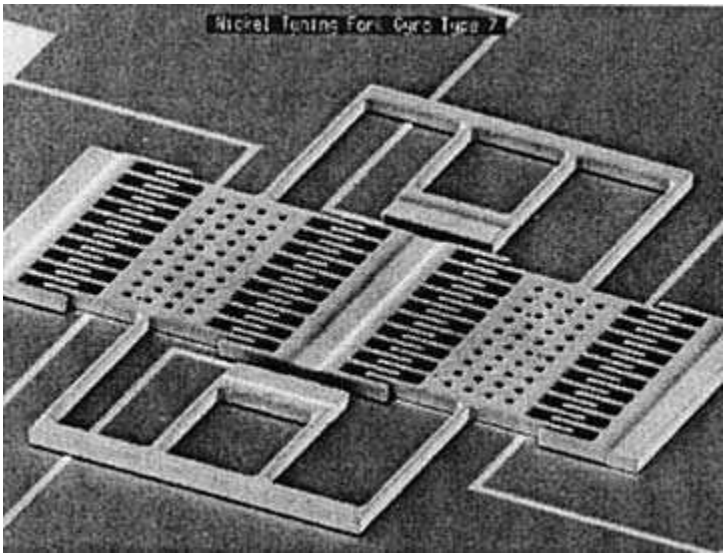


Fig. I.14 Comb drive tuning fork gyroscope develop by Draper Lab in Cambridge [5]

The MPU6050 sensor is 3-axis gyroscope, 3-axis accelerometer in a 4x4 package. The MPU-6050 is designed for the low power, low cost and high-performance requirements for wearable devices. It has an I2C interface and in the project scope it can be placed on the main PCB or it can be placed on an external PCB and connected through an external connector. This solution was adopted because in the beginning of the design, the location of the ePC was not confirmed to be inside of the VR casing, but the gyro should always be on the user head to track his movement. The I2C bus must be pulled up with the same voltage of the signal logic.

2. Radio Frequency (WIFI/BT)

Wi-Fi is the technology for wireless local area networking with devices based on the IEEE 802.11 standards. Devices that can use Wi-Fi technology include personal computers, video-game consoles, smartphones and tablets, smart TVs and modern printers. Wi-Fi compatible devices can connect to the Internet via a WLAN and a wireless access point. Such an access point has a range of about 20 meters indoors and a greater range outdoors. Hotspot coverage can be as small as a single room with walls that block radio waves, or as large as many square kilometers achieved by using multiple overlapping access points. Wi-Fi most commonly uses the 2.4 gigahertz (12 cm) UHF and 5.8 gigahertz (5 cm) SHF ISM radio bands. Anyone within range with a wireless network interface controller can attempt to access the network; because of this, Wi-Fi is more vulnerable to attack than wired networks.

The project needs to have a WIFI/BT feature because the BT can provide compatibility with all kind of controllers in the market and is widely spread and WIFI is used to download and update the VR content. The two technologies are complex and are beyond the scope of this thesis. The VR goggles incorporate a WIFI SoC architecture because designing the RF solution is complex and prone to errors, so an already integrated solution is preferable. The chip needs an external 37.4 MHz crystal and several power tuning components. It provides support for WIFI and BT through 3 antennas. The design discussion about this subject remains about the layout of antennas and will be covered in chapter 7 of PCB Layout.

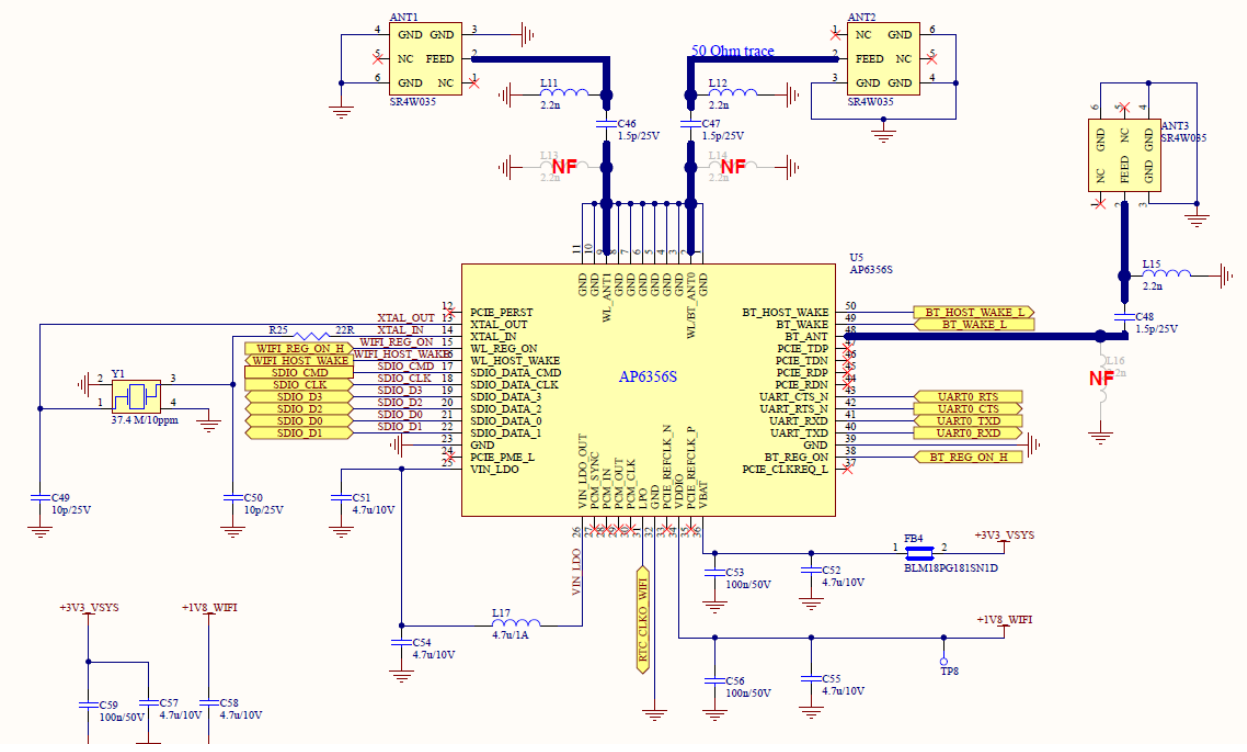


Fig. I.15 WIFI/BT schematics

3. Power Management

The system can be powered from two sources:

- Type-C cable plugged in PC or socket
- Battery

To be able to support two power paths, a power management architecture was implemented. Also, the system itself needs to be able to charge the attached battery. The PMIC should be able to choose from the two power sources. If the battery is not charged enough to power the system, the PMIC should charge it and in the same time provide direct power for the system. The USB Type-C Power delivery can provide a maximum of 15W (5V @ 3A) through VBUS line.

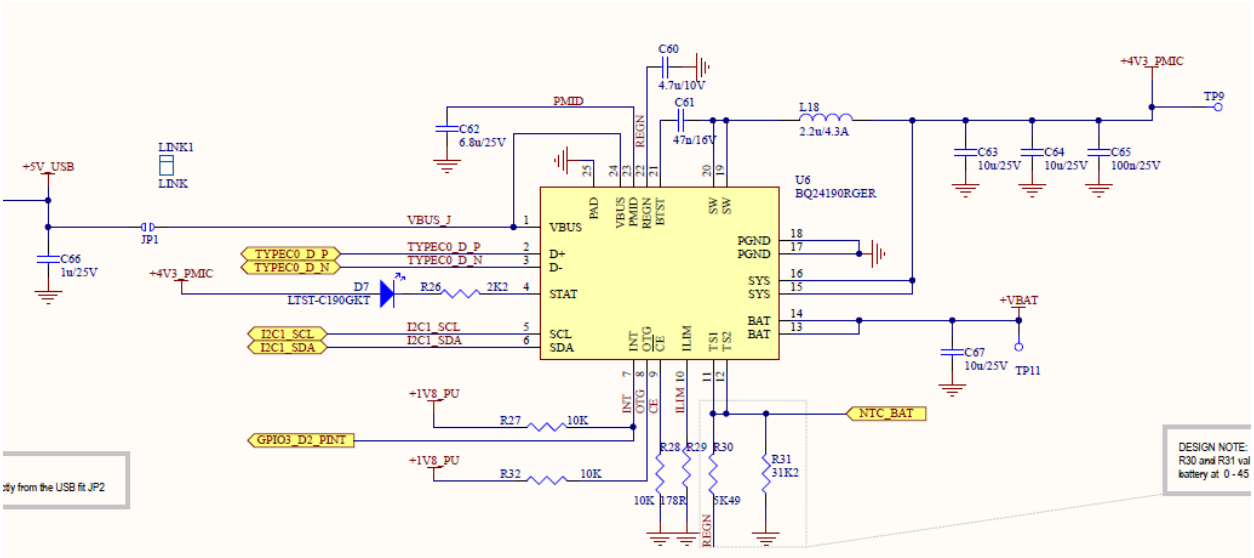


Fig. I.16 Power management IC schematic

PMIC

BQ24190 TI chip was chosen to manage the power. It can support an input voltage between 3.7 and 17V and an input current of 3A. The chip has a safety level regarding the input maximum current as it can be set by software and limited by hardware by putting a series resistor on the ILIM pin. The resistor value can be calculated with the equation below:

$$I_{INMAX} = \frac{1\,V}{R_{ILIM}} \times 530$$

On the output it can provide for the battery a maximum charging current of 4.5 A (fast-charge). The peak current discharged from battery can top 9A, but the continuous mode can provide 6A which is more than the system will need. The efficiency is above 90%. The maximum output voltage is 4.3V so after this stage a boost converter is needed.

The charging operation is a delicate one because the battery can get damaged and can heat up to an extent where it could catch fire or worst, explode. The bq24190 continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the VLTF to VHTF thresholds. During the charge cycle the temperature must be limited between the VLTF and VTCO thresholds, else the device suspends charging and waits until the battery temperature is within the normal range. Figure 17 illustrates better these phases.

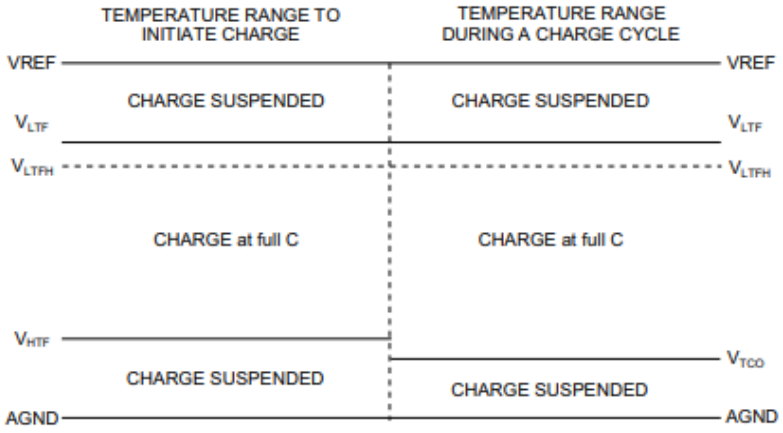


Fig. I.17 Thermistor sense thresholds (bq24190 datasheet)

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1\right)}$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,
RTH_{COLD} = 27.28 kΩ
RTH_{HOT} = 4.911 kΩ
RT1 = 5.52 kΩ
RT2 = 31.23 kΩ

When a heating problem occurs, the STAT LED starts to blink and an interrupt is send to the CPU.

Boost converter

The boost converter used is 98% efficient for converting 4.3V in 5V at 3A. The main advantage of this chip is that it has a constant current feature. When the current demand increases the boost will enter in the constant current mode to provide same power to the system. Otherwise the chip operates in constant voltage state.

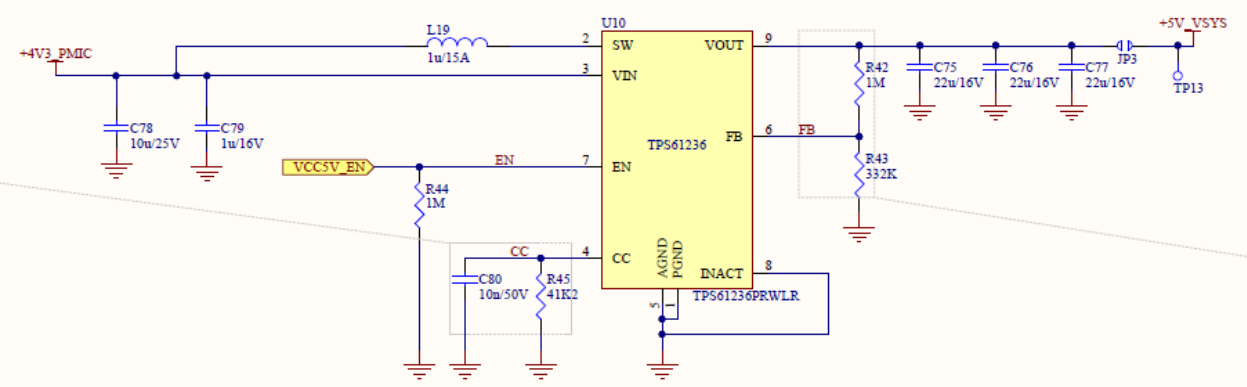


Fig. I.18 Boost converter schematic

The battery state-of-charge needs to be monitored. A sensing circuit is implemented to communicate with the CPU the battery level through I2C bus.

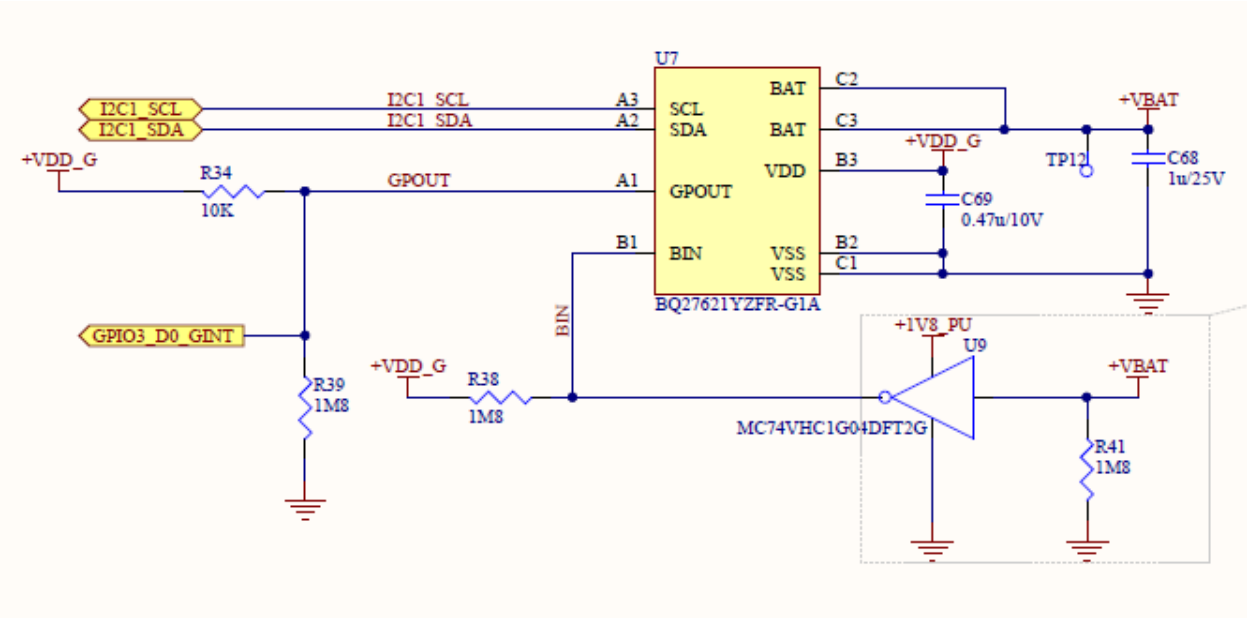


Fig. I.19 Battery sensing schematic

3.1. Battery

The power subject is an important one. The battery played a very important role in determining the form factor and the power-on time, which are among the most important topics of this project. The battery should last at least 1.5 hours of intense GPU and CPU high loads. To roughly estimate what the power consumption will be, a development board with the same CPU was bought and several tests were performed on it consisting in a demo content, close in performance demanding with the actual VR applications that will be rendered on the goggles.

Fig. I.20 Boot-up power consumption

After the test were performed, it was found that the maximum power drawn was 12W. For a safe operational runtime, the system should have a protection margin of at least 20%. So, in the end the battery should provide roughly 15W for at least 1.5 hours. In energy, this means:

$$15W \times 1.5h = 22.5\,Wh$$

The system runs at 5V so if the total energy needed is divided by the voltage needed, results:

$$22.5Wh \,/\, 5V = 4500\,mAh$$

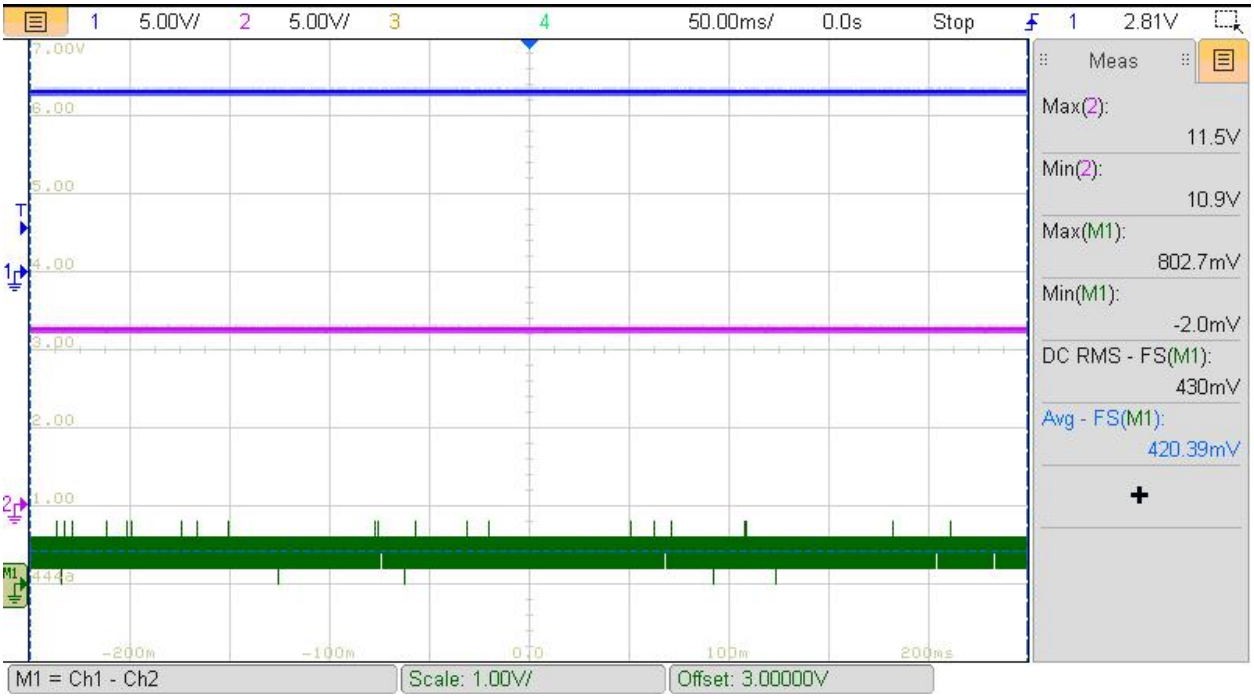


Fig. I.21 IDLE state power consumption

Fig. I.22 LOAD state power consumption

Fig. I.23 Shutdown power consumption

So, the battery needed must have at least 4500mAh. The current power market has different options for batteries regarding the number of cells (1,2,3 etc.) which influence the voltage rating because a standard cell is rated 3.7 V. The multi cell batteries have large form factors which excludes them. A single cell battery rated 3.7 is preferred. This means that is needed a battery with capacity of:

$$22.5Wh\ /\ 3.7V\ =\ 6000\ mAh$$

From this analysis it concludes that for a 1.5 hours of high load runtime a 3.7 @ 6Ah battery can sustain the needed power. All calculated values are true if we assume a 100% conversion efficiency of the power management ICs. In reality, the PMIC chose has a 92% efficiency rate @ 3A, combined with the regulator efficiency of 98% @ 3A. If we track back the losses in the power management modules we should add roughly 10% at the existing 15W. So, the real and safe power level should be 16.5W.

If the values are recalculated with this value it will result a needed battery of 3.7 @ 6700mAh, but this type of battery is hard to find on the market. Given the fact that the capacity increased only with 10% and also, remember that a safe margin was applied to the power requirement, it can be concluded that the 3.7@ 6000mAh should be safely used for 1.5 h runtime.

II. PCB Layout

1. EMC

When it comes to PCB layout design, there is a main goal to have in mind and try to achieve - EMC rules. The widespread use of electronic circuits for communication, computation, automation, and other purposes makes it necessary for diverse circuits to operate near each other. All too often, these circuits affect each other adversely. Electromagnetic interference (EMI) has become a major problem for circuit designers, and it is likely to become even more severe in the future. The large number of electronic devices in common use is partly responsible for this trend. In addition, the use of integrated circuits and largescale integration has reduced the size of electronic equipment. As circuitry has become smaller and more sophisticated, more circuits are being crowded into less space, which increases the probability of interference. In addition, clock frequencies have increased dramatically over the years—in many cases to over a gigahertz.

Electromagnetic compatibility (EMC) is the ability of an electronic system to:

- function properly in its intended electromagnetic environment and
- not be a source of pollution to that electromagnetic environment.

The electromagnetic environment is composed of both radiated and conducted energy. Therefore, has two aspects, emission and susceptibility.

Susceptibility is the capability of a device or circuit to respond to unwanted electromagnetic energy (i.e. noise). The opposite of susceptibility is immunity. The immunity level of a circuit or device is the electromagnetic environment in which the equipment can operate satisfactorily, without degradation, and with a defined margin of safety. One difficulty in determining immunity (or susceptibility) levels is defining what constitutes performance degradation. Emission pertains to the interference-causing potential of a product. The purpose of controlling emissions is to limit the electromagnetic energy emitted and thereby to control the electromagnetic environment in which other products must operate. Controlling the emission from one product may eliminate an interference problem for many other products. Therefore, it is desirable to control emission to produce an electromagnetically compatible environment. To some extent, susceptibility is self-regulating. If a product is susceptible to the electromagnetic environment, the user will become aware of it and may not continue to purchase that product. Emission, however, tends not to be self-regulating [6].

A product that is the source of emission may not itself be affected by that emission. To guarantee that EMC is a consideration in the design of all electronic products, various government agencies and regulatory bodies have imposed EMC regulations that a product must meet before it can be marketed. These regulations control allowable emissions and, in some cases, define the degree of immunity required. EMC engineering can be approached in either of two ways: one is the crisis approach, and the other is the systems approach. In the crisis approach, the designer proceeds with a total disregard of EMC until the functional design is finished, and testing—or worse yet—field experience suggests that a problem exists.

The systems approach considers EMC throughout the design. The problems are anticipated at the beginning of the design process and this way the EMC becomes a part of the whole system from electrical, mechanical and even software consideration. As a result this approach the EMC considerations are built in the product and not added onto. This is the most desirable approach in terms of low costs - money or time.

The proper design and layout of a printed circuit board can mean the difference between the product passing or failing EMC requirements. Such things as component placement, keep out zones, trace routing, number of layers, layer stackup (order of layers and layer spacing), and return path discontinuities all are critical to the EMC performance of the board.

The thesis will discuss each one of them and keeping in mind the project requirements and constraints described previously.

2. Noise

Noise is any electrical signal present in a circuit other than the desired signal. This definition excludes the distortion products that are present in a circuit due to nonlinearities. Although these distortion products may be undesirable, they are not considered noise unless they are coupled into another part of the circuit. It follows that a desired signal in one part of a circuit can be noise when coupled to some other part of the circuit. Noise sources can be grouped into the following three categories:

- intrinsic noise sources that arise from random fluctuations within physical systems, such as thermal and shot noise;
- man-made noise sources, such as motors, switches, computers, digital electronics, and radio transmitters;
- noise caused by natural disturbances, such as lightning.

Interference is the undesirable effect of noise. If a noise voltage causes improper operation of a circuit, it is interference. Noise cannot be eliminated, but interference can. Noise can only be reduced in magnitude, until it no longer causes interference.

2.1. Common mode noise

The USB 2.0 data signals can reach frequencies up to 240 MHz. However, fast transition times and long lines may induce radiations due to common mode noise. To avoid these issues, the most efficient device to reduce problems is a common mode filter.

In the picture below is presented how the noise appears in differential pairs due to the skew between them. This is the noise that can radiate and produce trouble in the system.

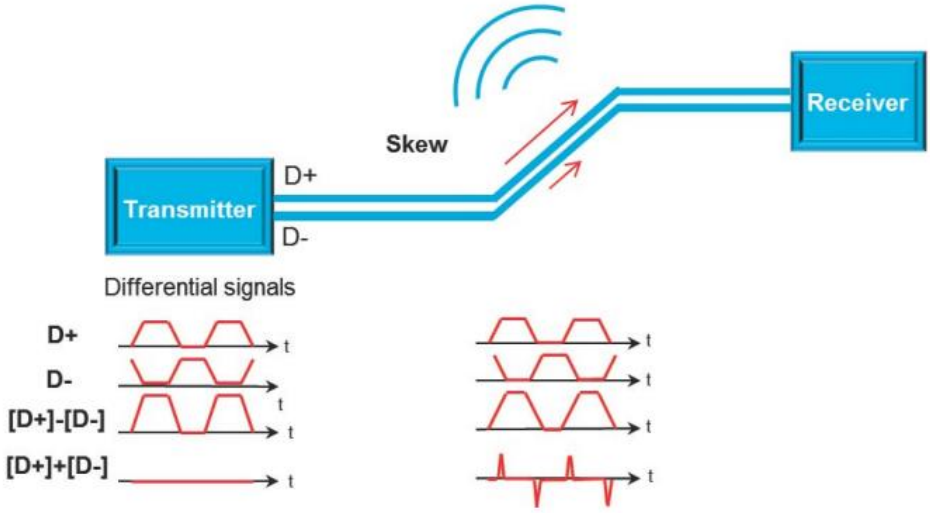


Fig. II.1 Noise emissions

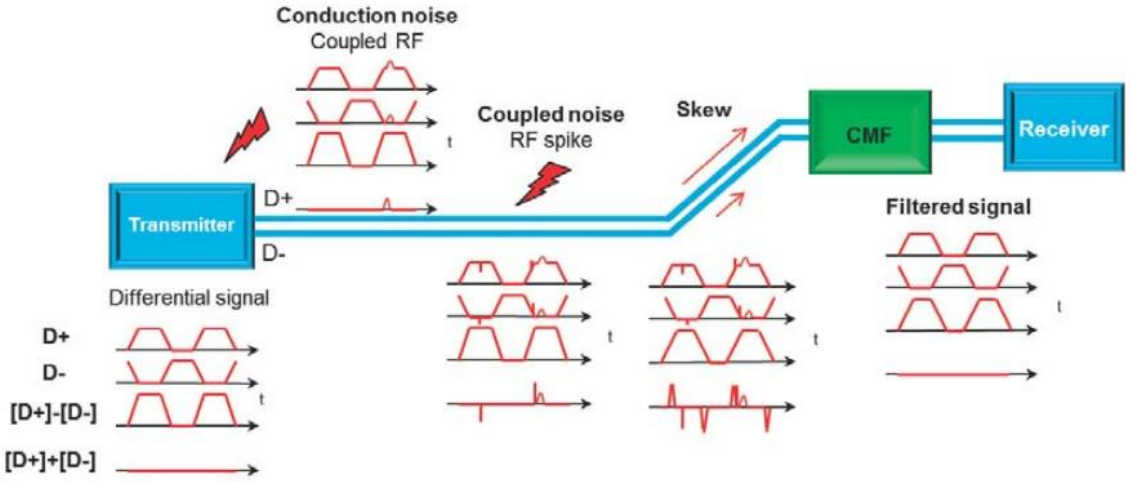


Fig. II.2 Noise filtered with CMF

After CMF is introduced, the signal is filtered as shown in the figure 2.

2.2. Common mode filter

In this type of filter, two coupled inductors are present:

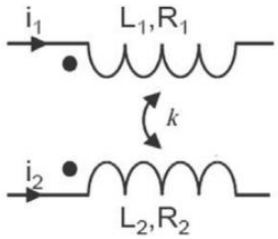


Fig. II.3 CMF equivalent circuit

The couple coefficient is called k. If L_1 and L_2 are two inductance values and M the mutual inductance, the following equation is given:

$$k = \frac{M}{\sqrt{L_1 \times L_2}}$$

If I_1 and I_2 are the currents flowing to each inductor, and R_1 and R_2 their DC resistance, their impedances are as follows:

$$Z_1 = R_1 + j\omega L_1 + j\omega M \times \frac{I_2}{I_1}$$

$$Z_2 = R_2 + j\omega L_2 + j\omega M \times \frac{I_1}{I_2}$$

If L_1 and $L_2 = L$ and $k \approx 1$:

$$M = k \times \sqrt{L_1 \times L_2}$$

$$M = L$$

In differential mode $I_2 = -I_1$

$$Z_1 = R_1 + j\omega(L_1 - M)$$

$$Z_2 = R_2 + j\omega(L_2 - M)$$

So, as the equation describes, the filter presents a low resistive impedance equal to DC resistance of the inductances therefore there is a low attenuation of the high-speed differential signal.

Having a wide range of filters available on the market for different application, the main parameter that I researched is the insertion loss. Based on datasheet I chose the ACM2012-900-2P and I investigated the propagation properties using the S-parameters in Ansoft Designer SV.

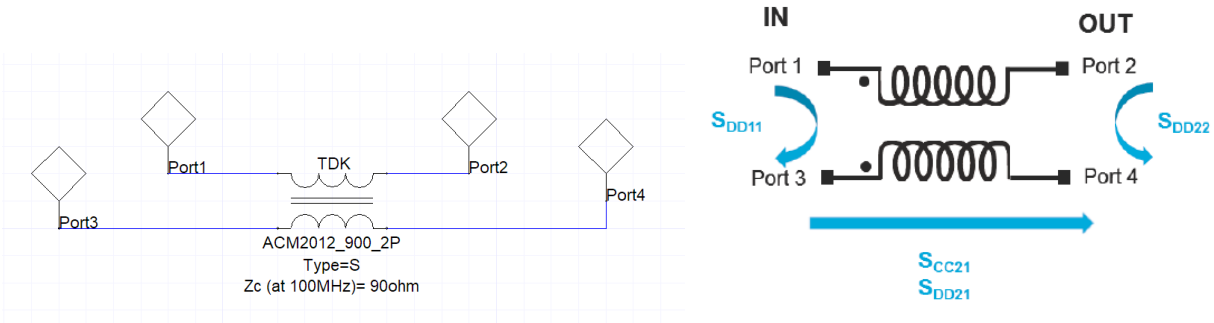


Fig. II.4 Ansoft two-port representation

Two main parameters are defined:

• SCC21 common mode rejection, the filter efficiency cuts the unwanted noise in a specific frequency range;
• SDD21 defines the differential bandwidth of the filter, the filter ability to drive the main signal without distortion;
• SDD11 and SDD22 defining the differential return losses of the filter;

These four characteristics, called mixed-mode S parameters, are calculated by S parameter results of two-port measurements.

Equations for all parameters mentioned above are:

• $SCC_{21} = 0.5 \times (S_{21} + S_{23} + S_{41} + S_{43})$
• $SDD_{21} = 0.5 \times (S_{21} - S_{23} - S_{41} + S_{43})$
• $SDD_{11} = 0.5 \times (S_{11} - S_{13} - S_{31} + S_{33})$
• $SDD_{22} = 0.5 \times (S_{22} - S_{24} - S_{42} + S_{44})$

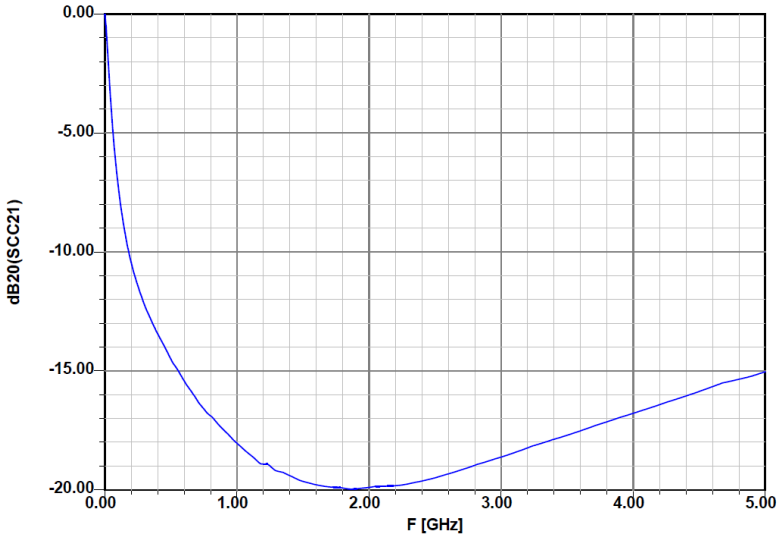


Fig. II.5 Common mode rejection

Figure 5 shows the typical common mode rejection. In this curve, the maximum rejection level of -20 dB is achieved at 2 GHz, the rejection range is wide, and this is needed to eliminate the unwanted harmonic, which can disturb some systems. To keep the integrity of the differential signal, SDD21 parameter must be considered and the lower attenuation improves the bandwidth. This parameter is measured at -3dB (see figure 6). From this graph the bandwidth is proper for a USB 2.0 application.

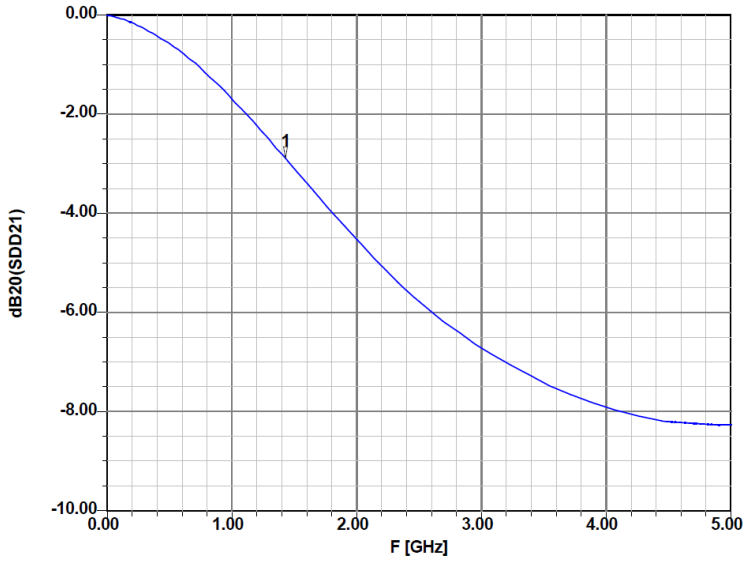


Fig. II.6 Differential bandwidth

After presenting all the arguments how the common mode filter was chosen, I can conclude that this was the best solution to avoid issues like common mode noise induced by radiated or conducted RF or skew between tracks. Also, it allows a system to improve its EMI robustness.

2.3. PI filter

Another type of noise that can escape through USB connector and cause EMI problems is the power rail noise on the USB power line. To prevent this, I choose to use a PI filter which have many advantages also for other roles not just for filtering noise picked up over the length of the cable. The capacitors that form the PI filter keep the VCC voltage from dropping low enough to reset the USB devices whenever a new USB device is plugged in. Also, the inductive component on the PI filter is not a regular inductor but a ferrite bead that will keep the inrush current within the spec. Also, it decouples the power rail, ensuring that the device itself does not feed noise back to the USB source.

An important issue affecting the final performance of the filter is the right selection of capacitors and ferrite bead. For high frequency attenuation, capacitors with low ESL and low ESR for ripple current capability must be selected. To achieve low ESR and ESL the output capacitor could be split into different smaller capacitors put in parallel to achieve the same total value. Filter inductors should be designed to reduce parasitic capacitance as much as possible, the input and output leads should be kept as far apart as possible.

3. ESD

When it comes to external connectors another problem arises, the electrostatic discharge. ESD is the accumulation of positive or negative charges on insulators or conductors. These charges can vary, based on the stored capacitance of certain items with respect to an object having a corresponding opposite charge. The word static simply means the charge cannot be equalized or transferred through electromotive force until there is a decrease in the capacitance between two objects. The interfaces need to be protected against ESD because high voltages can penetrate through this port. Therefore, the ESD that enters the device must find a safe way to escape to ground. If there are not any protective devices than this, high voltage of several thousand volts will discharge directly to the internal ICs. Under the normal drive voltage (several volts), the IC is isolated from ground, so data communication is not impaired. The ability to ground an IC circuit when several thousand volts are applied to it, and also to isolate it from ground is necessary to use an ESD protective device [7].

The following graph shows the difference between the voltages at the IC side depending upon whether an ESD protective device is installed. Here, an 8 kV ESD is generated using an ESD gun and the voltage after it has passed through the device is measured using an oscilloscope. From the waveform of the graph, the existence of the ESD protective device greatly reduces the voltage applied to the IC side.

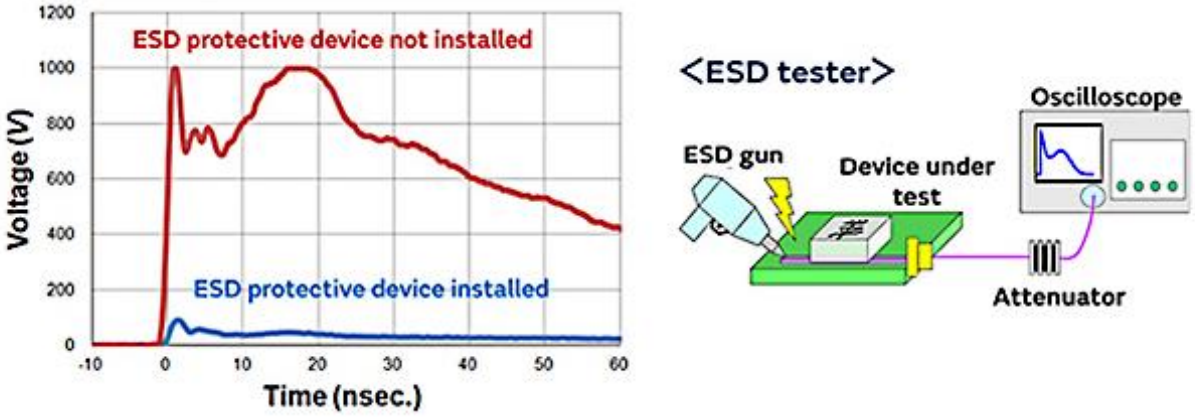


Fig. II.7 ESD discharge

The discharge waveform is used to evaluate the performance of the ESD protective device. In the graph, the value of the peak voltage immediately after the application of ESD is called “peak voltage” and the value 30 ns later is called “clamp voltage”. The graph shows that the lower the values of peak and clamp voltages, the higher is the ability of the ESD protective device to protect a product. The lower these values and the smaller the area of the waveform of the product, the smaller will be the damage applied to the IC side.

The ESD protection is divided in 4 levels of intensity. For the current application it was chosen level 4, the highest level of protection. The table in figure 9 describes the standard values for each level.

In figure 8 is the characteristic of the device used to protect the USB lines. ESDR0502N device will protect the USB connections (VCC, D+, D−, and GND) of one USB port. When the voltage on the data lines exceeds the bus voltage (plus diode voltage drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode suppresses ESD strikes directly on the voltage bus and directs the surge to ground, protecting both the power and data pins.

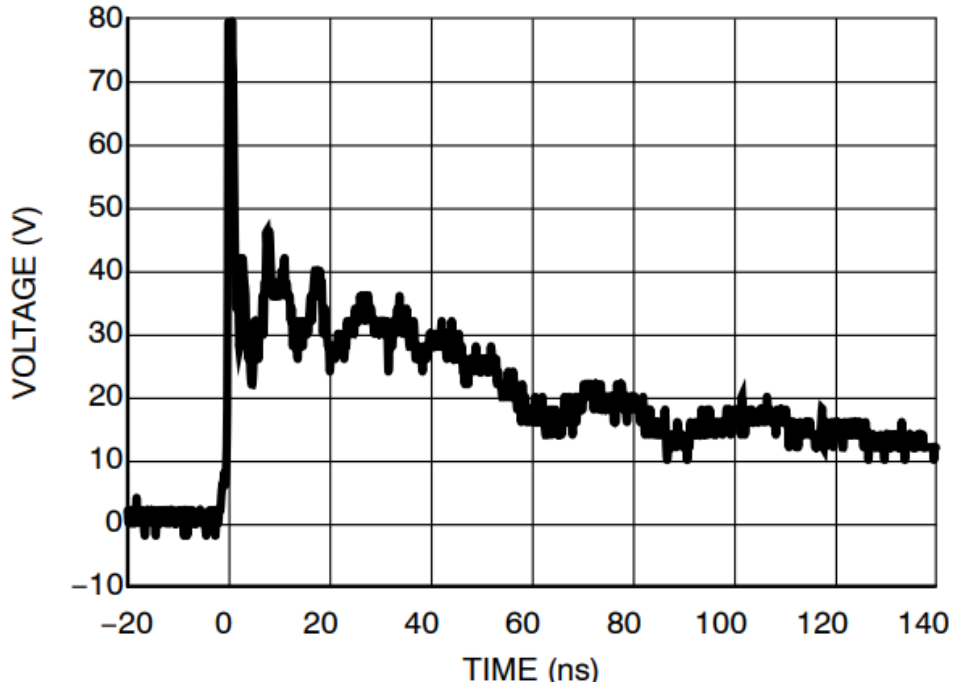


Fig. II.8 ESD clamping voltage (source: Littlefuse)

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

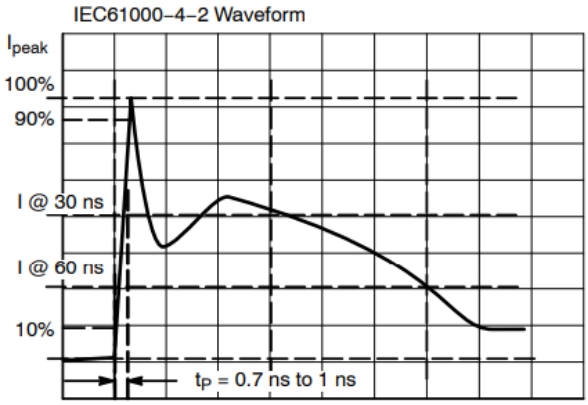


Fig. II.9 IEC ESD standard specifications (source: Littlefuse)

An important parameter of the ESD protection device is the line added capacitance which can degrade the integrity of the data signal if is not properly chosen. Capacitance is nonlinear with respect to signal frequency. In other words, as the signal frequency increases, the capacitance effect (impedance) changes. If a mismatch occurs between the capacitance of a suppressor and the signal speed of a circuit, the signal (and its ability to properly transmit data) can be degraded.

The use of capacitance is a common technique for noise filtering. The parallel capacitor attenuates high frequency noise, while the circuit operates without disruption at lower frequencies. Conversely, a series capacitor will block low frequencies and pass high frequencies without attenuation or distortion. Suppressor capacitance is an important consideration since the suppressors are installed in parallel in the circuit that is to be protected. As the speed of a data stream increases, the amount of distortion will increase as a function of the device capacitance. As a result, high frequency signals can be "filtered" due to the capacitance of the suppressor. To avoid "filtering" or distortion of the signal, it is necessary to make sure that the capacitance of the suppressor is not too high for the data protocol.

Figure 10 illustrates the ESD capacitance effect on data lines. The CPU manufacturer advise for a capacitance lower than 0.5 pF. The actual device used, ESDR0502N, has a junction capacitance of 0.3 pF at 1MHz.

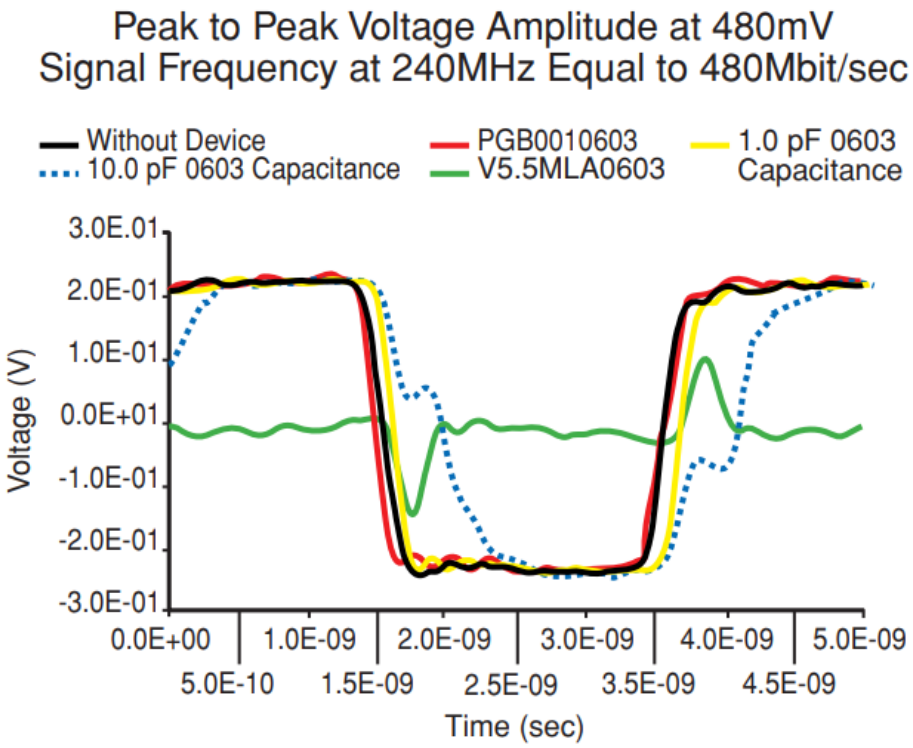


Fig. II.10 Signal integrity alteration (source: Littlefuse)

4. Layout Guidelines

4.1. Partitioning the PCB

First step while developing a PCB is to analyze the system that will be implemented and place the components in logic areas. If these areas are defined properly, 90% of the problems can be eliminated in the planning phase itself. Proper partitioning will minimize trace lengths, improve signal quality, minimize parasitic coupling, and reduce both PCB emissions and susceptibility [8].

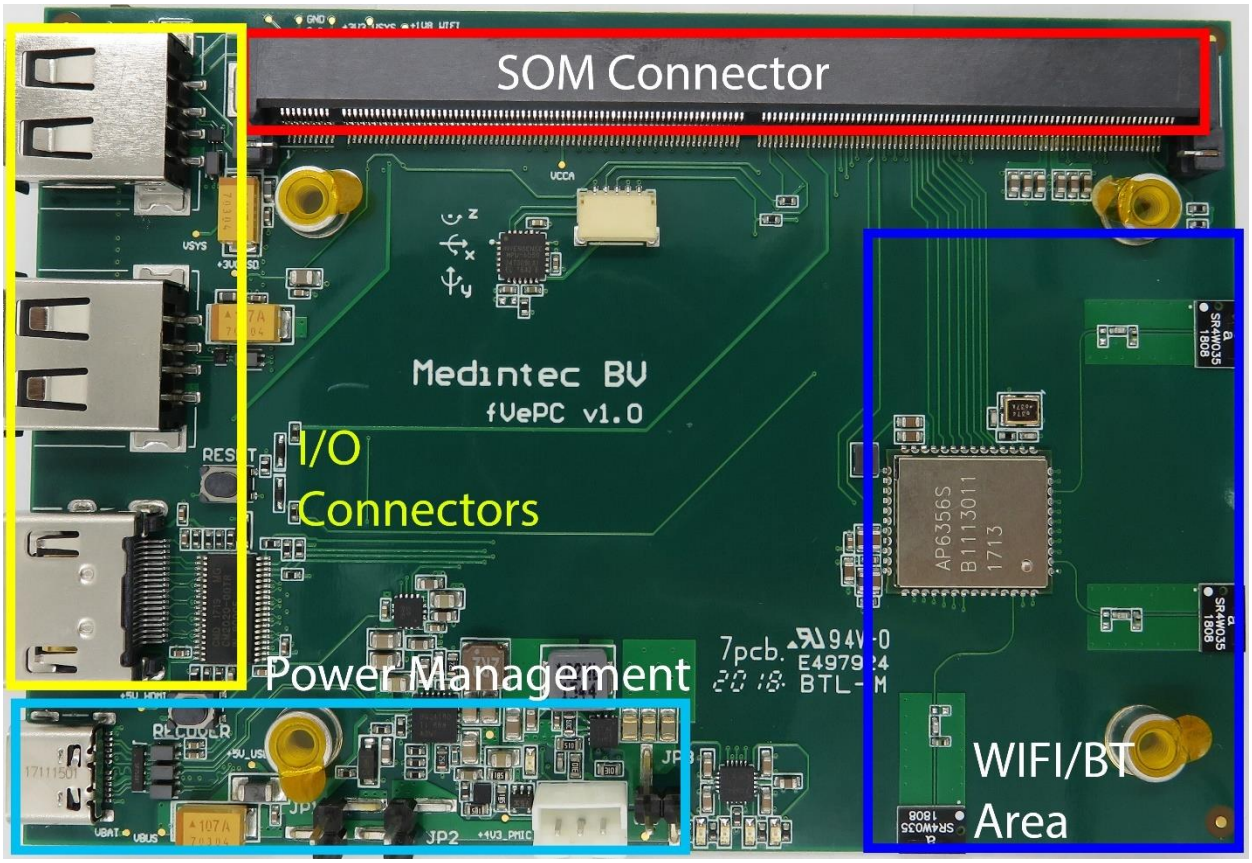


Fig. II.11 PCB functional blocks split

To ensure a proper functionality of the system the 3 main domains: high speed digital interfaces, power management and radio frequency modules must be separated. It can be seen that the main regions are clearly separated with one small exception, the USB Type-C connector. In the blue area, there is the power management chip that provides the needed voltage rails to the entire system. The power is supplied through the USB connector, but in case the system is powered from the battery and then the USB Type-C connection is used for data communication, the digital I/O signals mix-up with analog power signals. This means that in this area the power and ground planes need to be taken in discussion and used to separate the current flow from the two regions to not overlap on the same layer or to crosstalk on the adjacent one [9].

4.2. Return path discontinuities

One of the keys to determining the optimum printed circuit board layout is to understand how and where the signal return currents flow. The schematic only shows the signal path, whereas the return path is implicit. To address the above concern, one must remember how high-frequency return currents flow. The lowest impedance return path is in a plane directly underneath the signal trace (irrespective of whether this is a power or ground plane) because this provides the lowest inductance path. This also produces the smallest loop area. Because of the "skin effect" high-frequency currents cannot penetrate a plane, and therefore, all high-frequency currents on power and ground planes are surface currents. This effect will occur at frequencies above 30 MHz for 1-oz copper layers in a PCB. This means that a PCB manufacturing constraint arises. Copper thickness of the inner layers should be at least 1oz. Therefore, a plane is really two conductors. There can be a current on the top surface of the plane and there can be a different current, or no current at all, on the bottom surface of the plane. Major EMC, and signal integrity problems occur when there are discontinuities in the return current path. These discontinuities cause the return current to flow in large loops, which increases the ground inductance and the radiation from the board as well as increasing the crosstalk between adjacent traces and causing waveform distortion. In addition, a return plane discontinuity on a constant impedance PCB will change the characteristic impedance of the trace and produce reflections [10]. The three most common return path discontinuities that must be dealt with are as follows:

- Slots or splits in the power and/or ground plane;
- Signal traces changing layers, causing the return currents to change reference planes;
- Ground plane cut-outs around connectors, or under ICs;

Slot splits in planes

These types of splits are preferably to be nonexistent in a PCB, but there are scenarios where they can be eliminated and scenarios when they cannot.

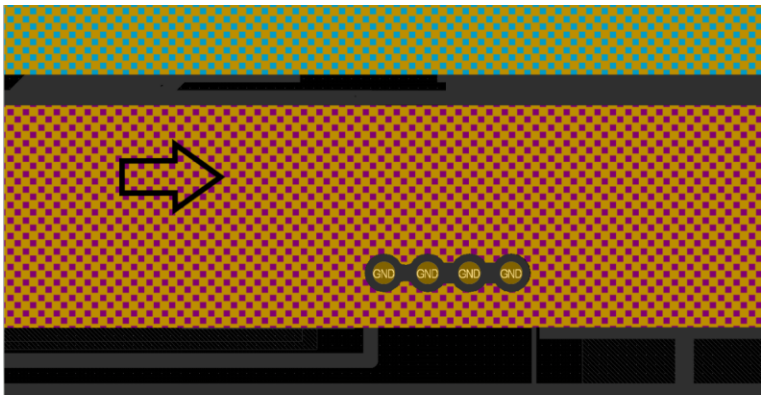


Fig. II.12 Current direction in slot split planes

The discontinuities due to vias can be seen here. There are not important since these are GND vias and the current flowing through the power plane is parallel with the split as shown by the arrow and no high-speed tracks are present in this area. Another problem can be caused by connectors with high density pins. In these cases, the GND plane is split by the vias (negative layer- bold color means plane discontinuity). This happens because on the top there are many signals that need to be fan-out from this area. In this case, it is safe because there are no high speed returning currents that need to pass through split area, connector being on the margin of the PCB.

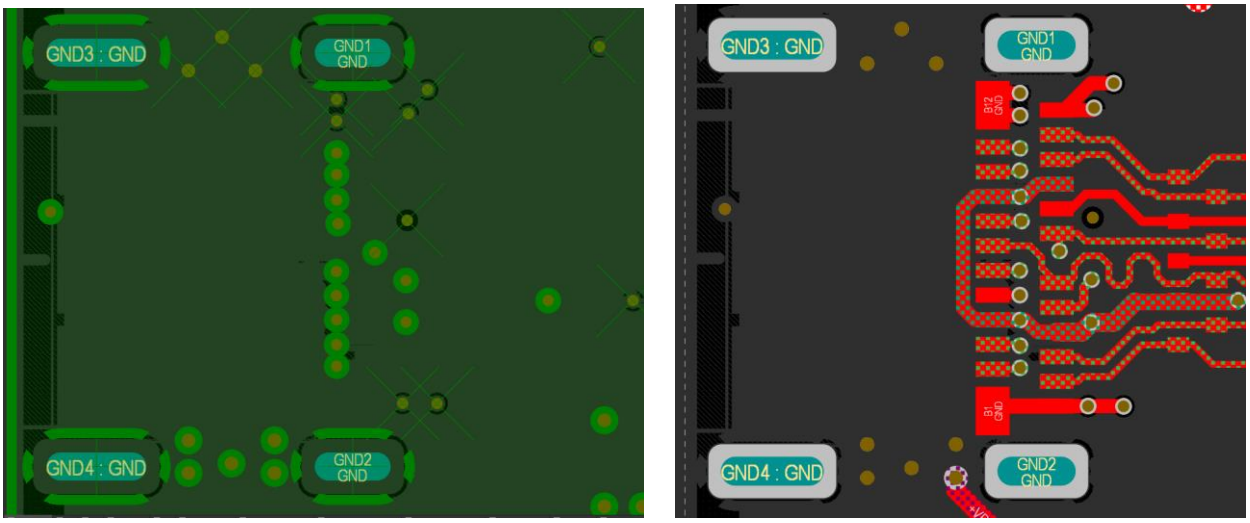


Fig. II.13 VIAs placement in the connector area

Placing the vias also on the other side of the connector was not possible because it is not recommended to place vias or track beneath the connectors that touch the PCB. There is just one via in that example because underneath the USB Type-C connector is the battery connector and the NTC connection should somehow be made. The via was tented, so no copper is exposed to the USB connector. Another example of keep-out area is beneath the SD card connector.

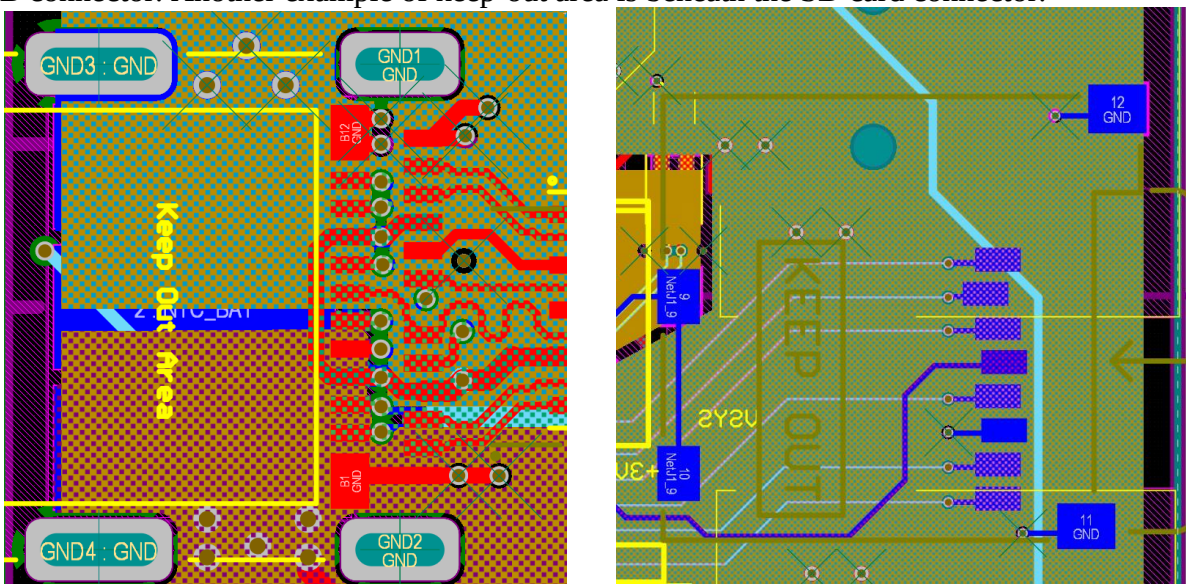


Fig. II.14 Keep-Out areas on the PCB

4.3. Changing reference planes

When a signal trace changes from one layer to another, the return current path is interrupted because the return current must also change reference planes. The question then becomes how does the return current flow from one plane to another? The return current will have to flow through the nearest decoupling capacitor, or plane-to-plane via to change planes. Changing reference planes obviously increases the loop area and is undesirable for all the reasons previously stated for split planes. Changing reference planes effectively adds impedance (inductance) in the return path. One solution to this problem is to avoid switching reference planes for critical signals (such as clocks), if possible. If there is a must to switch references from a power plane to a ground plane, then you can place an additional decoupling capacitor adjacent to the signal via to provide a high-frequency current return path between the two planes. This solution is not ideal, however, because this adds considerable additional inductance in the return path (typically about 5 nH). If the two reference planes are of the same type (either both power or both ground), then it can be used a plane-to-plane via (ground-to-ground, or power-to-power) instead of a capacitor immediately adjacent to the signal via. This approach is much better, because the added inductance (hence impedance) of a via is much less than that of a capacitor and its mounting. It is highly recommended that either a capacitor or via be added whenever critical signals change reference planes.

Whenever a signal switches layers and references first the top and then the bottom of the same plane, because of the skin effect, the current cannot flow through the plane; it can only flow on the surface of the plane. To drop a signal via through a plane, a clearance hole (anti-pad) must be provided in the plane, otherwise the signal would be shorted to the reference plane. The inside surface of the clearance hole provides a surface connecting the top and bottom of the plane and provides the path for the return current to flow from the top to the bottom of the plane as depicted in Fig. 15. Therefore, when a signal passes through a via and continues on the opposite side of the same plane, a return current discontinuity does not exist. This is, therefore, the preferred way to route a critical signal if two routing layers must be used. High-speed clocks and other critical signals should be routed (in order of preference) as follows:

- On only one layer adjacent to a plane.
- On two layers that are adjacent to the same plane.
- On two layers adjacent to two separate planes of the same type (ground or power) and connect the planes together with plane to plane vias wherever the signal trace changes layers.
- On two layers adjacent to two separate planes of different types (ground and power) and connect the planes together with capacitors whenever the signal trace changes layers, and hence reference planes.
- On more than two layers but is highly not recommended.

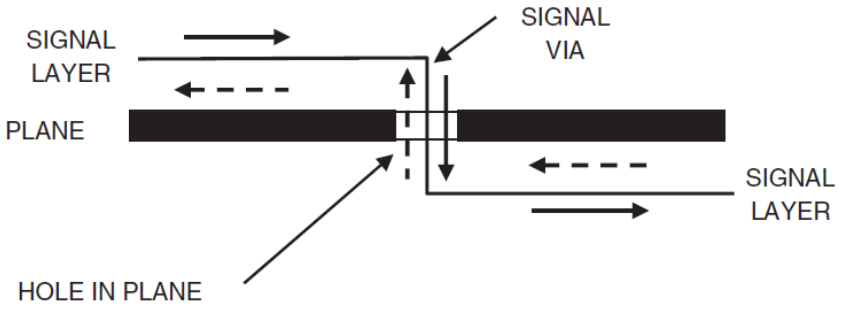


Fig. II.15 Same layer reference path current

In the project, connection on just one layer was used, the easiest and correct one, on two separated layers but with the same reference plane as in figure 16. (L4-GND-L6)

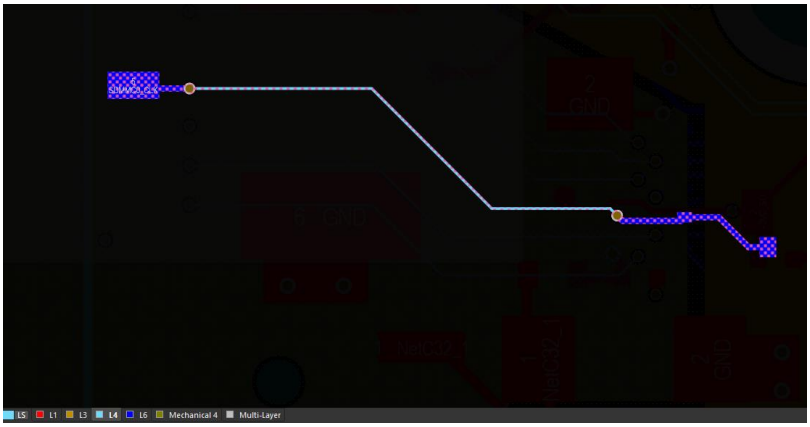


Fig. II.16 Routing example of signal on layers with adjacent reference plane

The second type of connection was made on 2 different layers but with the same type of reference plane (GND) that needs stitching vias

.

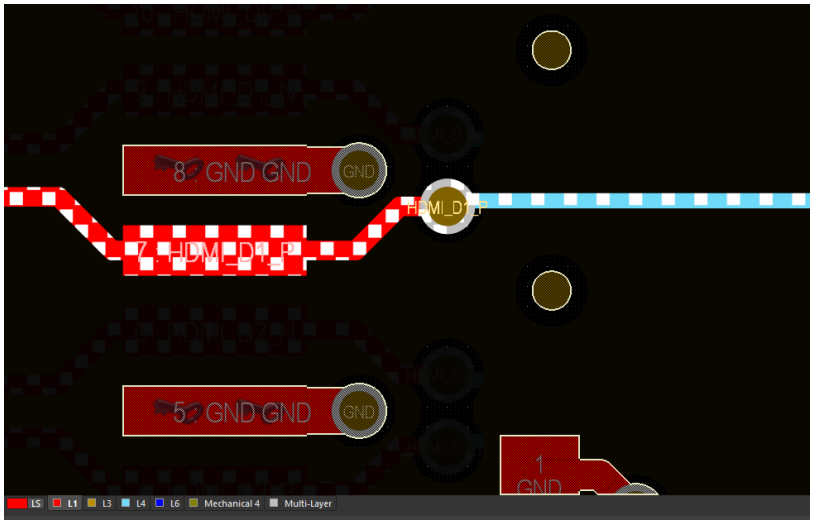


Fig. II.17 Stitching VIAs for return currents

5. PCB layer stackup

PCB layer stackup (the ordering of the layers and the layer spacing) is an important factor in determining the EMC performance of a product. A good stackup will produce minimal radiation from the loops on the PCB (differential mode emission), as well as the cables attached to the board (common-mode emission). However, a poor stackup will cause excessive radiation from both mechanisms.

The following four factors are important with respect to board stackup:

- The number of layers
- The number and types of planes (power and/or ground)
- The ordering or sequence of the layers
- The spacing between the layers

When using multilayer boards, six design objectives should be kept in mind, as follows:

1. A signal layer should always be adjacent to a plane.
2. Signal layers should be tightly coupled (close) to their adjacent planes.
3. Power and ground planes should be closely coupled together.
4. High-speed signals should be routed on buried layers located between planes. The planes can then act as shields and contain the radiation from the high-speed traces.
5. Multiple-ground planes are very advantageous, because they will lower the ground (reference plane) impedance of the board and reduce the common-mode radiation.
6. When critical signals are routed on more than one layer, they should be confined to two layers adjacent to the same plane.

Most PCB designs cannot meet all six objectives, so a compromise is required. For example, one is often faced with the choice between close signal to return plane coupling (objective #2) and close power to ground plane coupling (objective #3). Another choice is often between routing signals adjacent to the same plane (objective #6) or shielding signal layers by burying them between planes (objective #4). If the number of board layers permits, then one or the other of these objectives should be satisfied. From both an EMC and a signal integrity point of view, it is usually more important to have the return current flow on a single plane than to bury the signal layers between planes. Objectives #1 and #2 should always be achieved and not compromised.

In the current design all signals routing was done on 3 layers. To ensure a good EMC practice, power planes need to be interleaved between them to maximize the number of objectives presented. Objective #1 implies that the first layer needs the right beneath layer to be reference. We will assume the L2 as GND. The same reasoning applies for the bottom layer, so the last layer needs a GND reference layer above it. Right now, was added 2 GND planes to achieve the objective #1. This stackup is shown in figure 18.

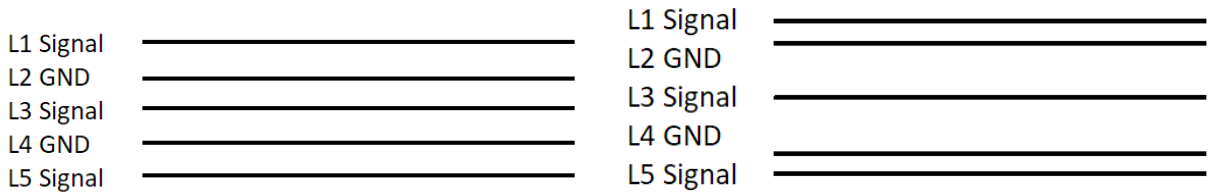


Fig. II.18 PCB stackup for #1 and #2

With this stackup if the distance between layers is changed, the #2 objective can be achieved also. Putting the reference planes near the top and bottom signal layers results in layer L3 signal needing a reference plane tightly coupled. Appears the need to use another layer to complete the #2 objective. In figure 19 another layer L3 PWR is added.

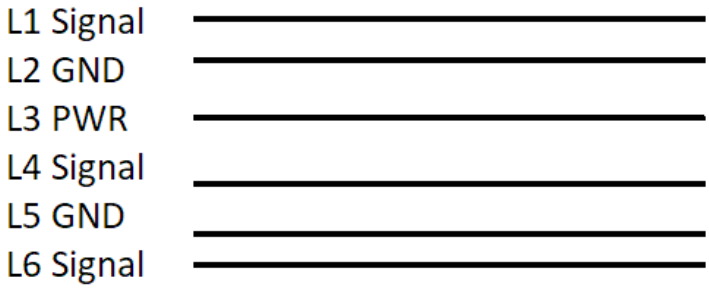
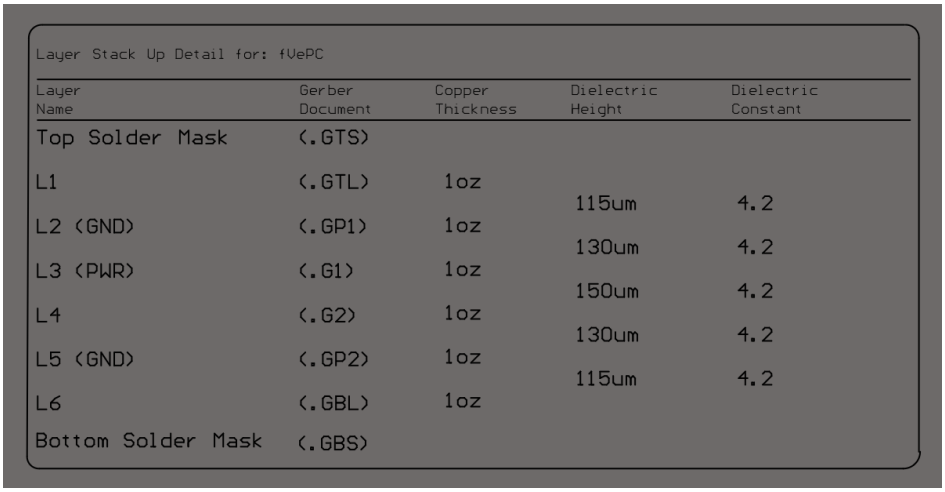


Fig. II.19 Stackup for #3 (the 6th layer is added)

With the 6th layer added the first two objectives are achieved. The #3 objective is completed by default with the current stackup and for the #4 objective only the L4 is confined between reference planes so let assume there is a part of it which is taken into consideration. Trying to achieve other objective it means to improve the number of layers to at least 10. This increase will have impact in the weight of the PCB but most important in the manufacturing costs. In the end the 6-layer stackup can provide a good EMC performance vs costs.

The final stackup developed by the rules presented above and sent for the manufacturing is shown in figure 20.



Layer Stack Up Detail for: fVePC

Layer Name	Gerber Document	Copper Thickness	Dielectric Height	Dielectric Constant
Top Solder Mask	(.GTS)			
L1	(.GTL)	1oz		
			115um	4.2
L2 (GND)	(.GP1)	1oz		
			130um	4.2
L3 (PWR)	(.G1)	1oz		
			150um	4.2
L4	(.G2)	1oz		
			130um	4.2
L5 (GND)	(.GP2)	1oz		
			115um	4.2
L6	(.GBL)	1oz		
Bottom Solder Mask	(.GBS)			

Fig. II.20 Real stackup used (manufacturing details)

6. High-Speed interfaces layout

The high-speed interfaces signal in this project are the HDMI, USB2.0, USB3.1 and SD card. These traces must be designed strictly by differential pair rules requirements. The turning corners of signal traces should be as far as possible with arc or obtuse angle, not a right angle or acute angle. In order to suppress EMI, the signals are recommended to be placed on the inner layer and ensure the reference plane is continuous and complete, otherwise, it will cause discontinuities in the traces impedance and increase the external noise.

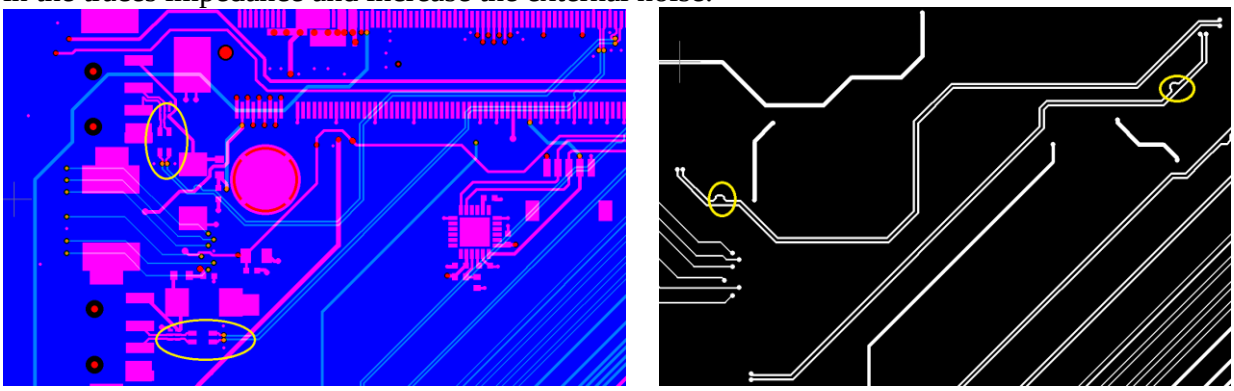


Fig. II.21 Challenging areas of USB 2.0 layout

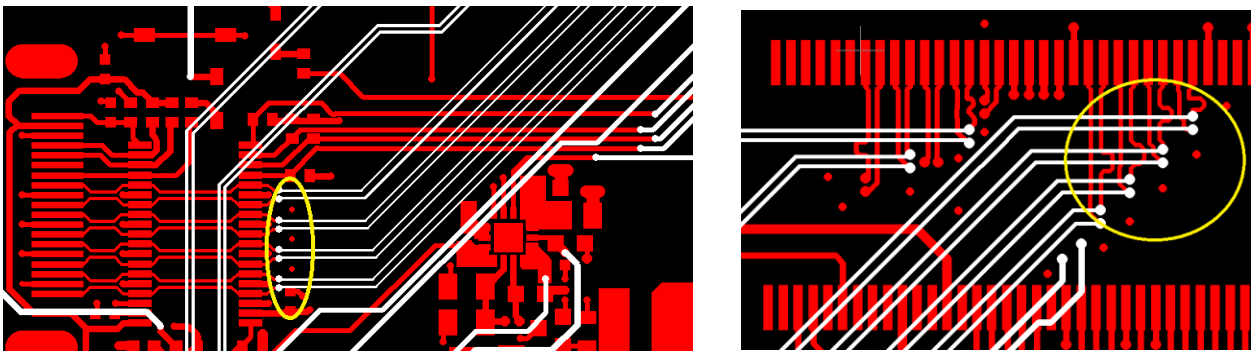


Fig. II.22 Challenging areas of HDMI layout

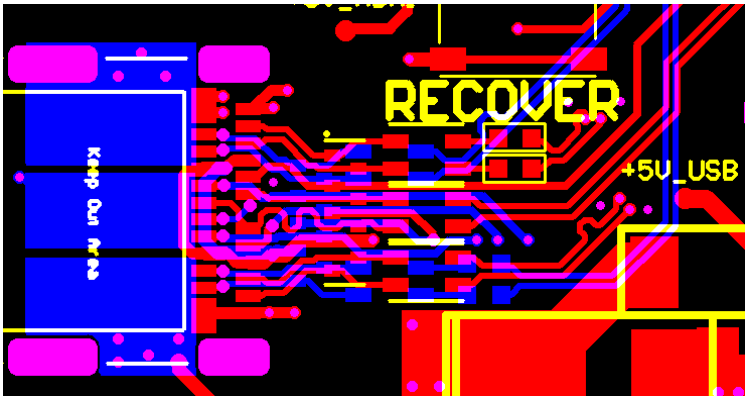


Fig. II.23 Challenging area of USB Type-C layout

In figure 24 the USB 2.0 ESD protection and common mode filter are marked. The signals start on the top layer with reference on L2 (GND). When the signal changes layer to L4 the reference layer changes also to L5 which is a GND plane. To preserve the current return path stitching vias are placed near the signal vias. When the signals return on top layer again, the stitching vias must be present nearby.

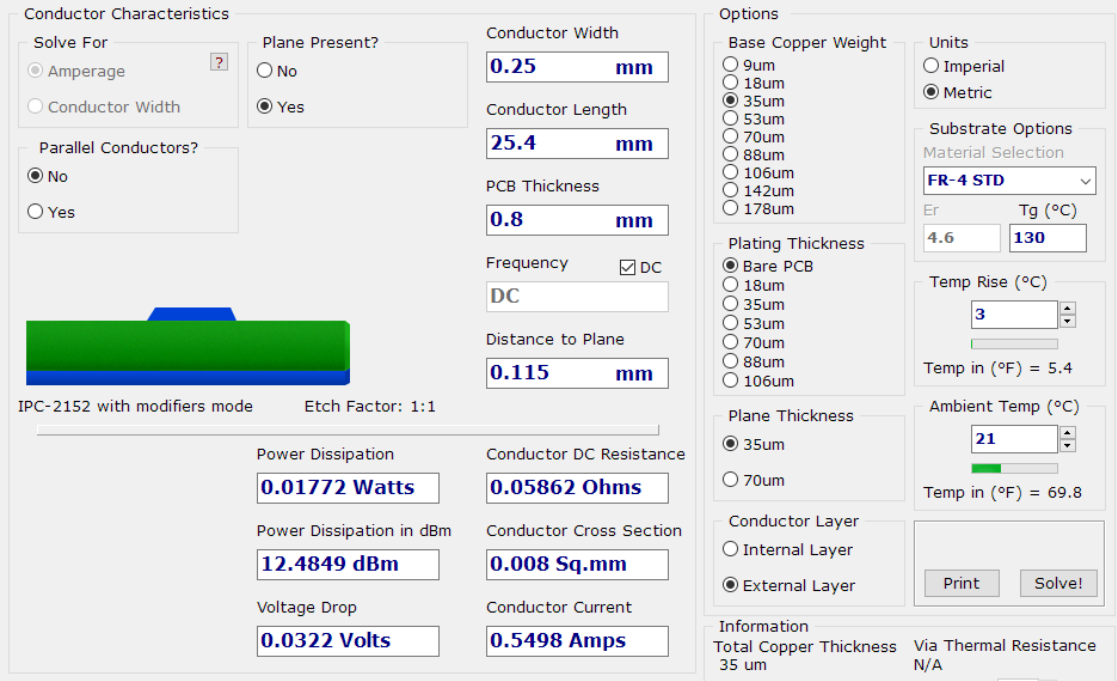


Fig. II.24 USB 2.0 power track width calculator (Saturn PCB Toolkit)

The power tracks width for USB is calculated to drive the maximum current drawn by this interface, 500mA. For a width of 250µm, the conductor can support 550mA with a temperature increase of only 3°C.

Another issue that need to be addressed is the signal pair skew difference. This translates in the track length differences which in this case were routed by 10% tolerance. The marked meanders in figure 21 are included to make the differential pairs equally and are introduced near where the imbalance in length is created, to ensure an equal propagation phase and to maintain a proper impedance of the track. The signal tracks width is also designed by the 90-ohm impedance matching that is specified by the CPU manufacturer. For the HDMI the manufacturer recommends a 100-ohm impedance track.

Another factor which determines the signal quality is represented by the stubs and vias number. A stub is a part of the track that splits the main current way. In figure 25, the first case presents a stub while the second method presents how it should be done when is needed to introduce a discrete component into the transmission line without affecting the signal integrity.

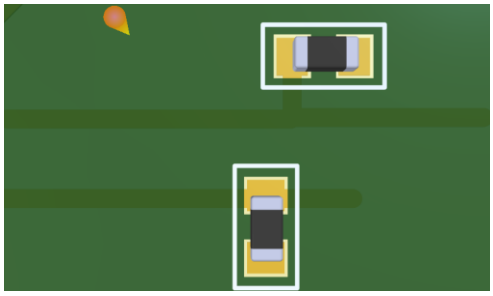


Fig. II.25 Incorrect vs Correct placement of passive components for data lines in high speed design

An unwanted stub can be created with a via if switching layers is done in an inappropriate way. If the back-drill manufacturing method is not used, then changing layers in high speed signals (USB, HDMI) should be done to minimize the stub length which will affect the signal quality. From top layer to minimize the via stub the best method is to go to the bottom layer and to use the whole length of the via. The worst-case scenario is switching from L1 top layer to the layer L2 which is right beneath it. The stub is seen as an impedance disturbing the signal track.

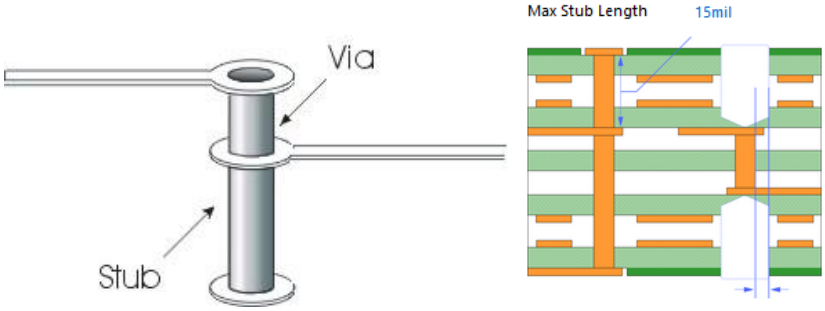


Fig. II.26 VIA stub

Maximum vias count is specified for every type of interface because the vias introduce also stray elements that influence the signal quality.

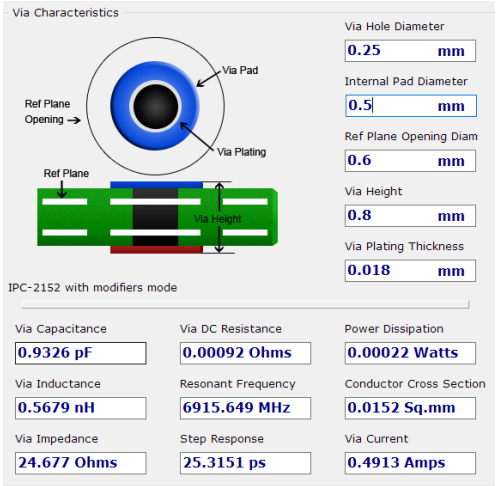


Fig. II.27 VIA electrical characteristics (Saturn PCB Toolkit)

Crosstalk

The problem in dense high-speed PCBs is that the space between 2 tracks can be very small. At the high speed the rising time of the signal can produce an undesired noise in the nearby signals which could alter the function of that circuit. The crosstalk is the voltage induced in a line by the adjacent lines. The magnitude of the crosstalk voltage is mainly determined by the adjacent signal rise times. If the signal rise time is short, it produces a lot of coupled voltage. Another factors that are influencing it are the coupled length, the distance between two tracks and how long they run in parallel. To keep crosstalk at minimum values the rise time of the signals should be increased, the distance between the tracks also increased as much as possible and the couple distance as short as possible. [11]

This unwanted phenomenon can be present not only for nearby tracks on the same layer, but also for the tracks on adjacent layers that run in parallel. To reduce the effect, orthogonal routing is recommended.

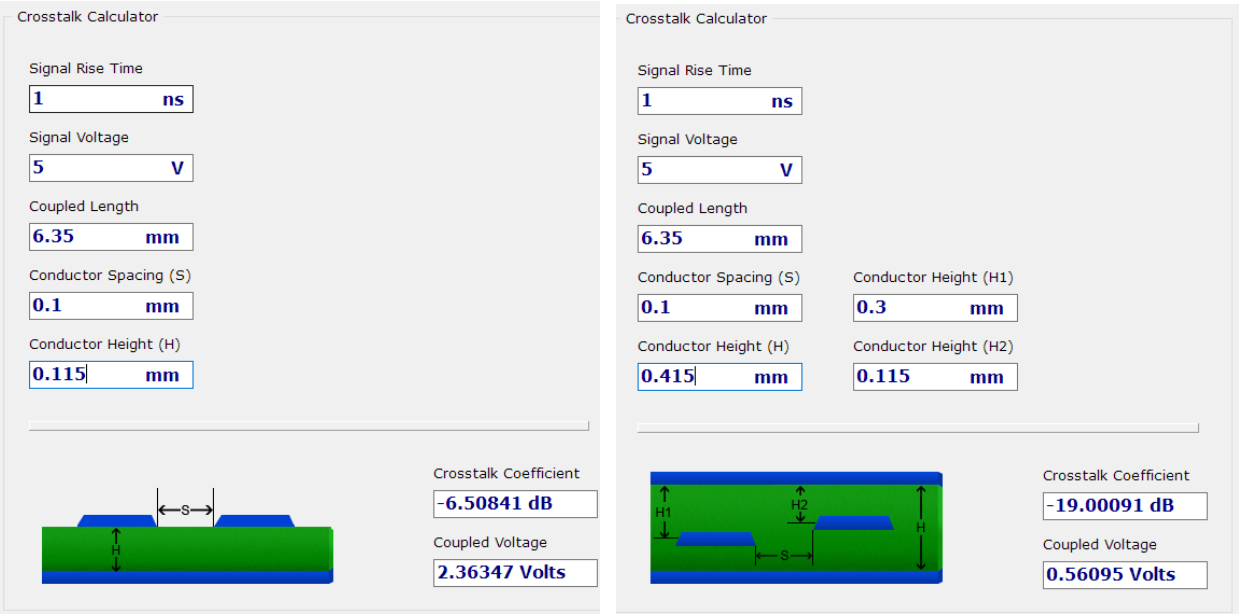


Fig. II.28 Crosstalk calculator (Saturn PCB Toolkit)

7. RF layout

Radio frequency module for WIFI and BT needs a 37.4 MHz crystal oscillator to be functional. The traces that connect the oscillator to the RF IC must be short and wide. Signals should not be routed under the oscillator because they can interfere through the crosstalk effect.

WIFI antennas placement is an important subject. The WIFI part can use a dual antennas setup and the BT one antenna. All functionality can be achieved with only one antenna for both, but for the best performance it is preferred that each function should have separate antennas. The traces that connects the IC with the matching circuit use rounded corners to minimize the line reflections. When it comes to the spacing between antennas, some myths suggest that antennas distances should be as big as possible to ensure that one of the antenna will not drop in the same null spot of the propagation wave that need to be received. The product will be used indoor, so there is hard to determine where the nulls will be found. A rule of a thumb suggests placing them ¼ or ½ lambda apart. [12] The wavelength of 2.4 GHz WIFI is around 12 cm. Considering that the PCB form factor is an important requirement placing them at ½ lambda is impossible. So, the antennas were positioned approximately at ¼ of wavelength apart. The antennas selected are SMD and need to be placed at the PCB margin far away from the PCB corners or other big metallic structures. Beneath the antennas there should be no copper to ensure a good propagation on all directions and to avoid to be shielded by the GND planes in the inner layers.

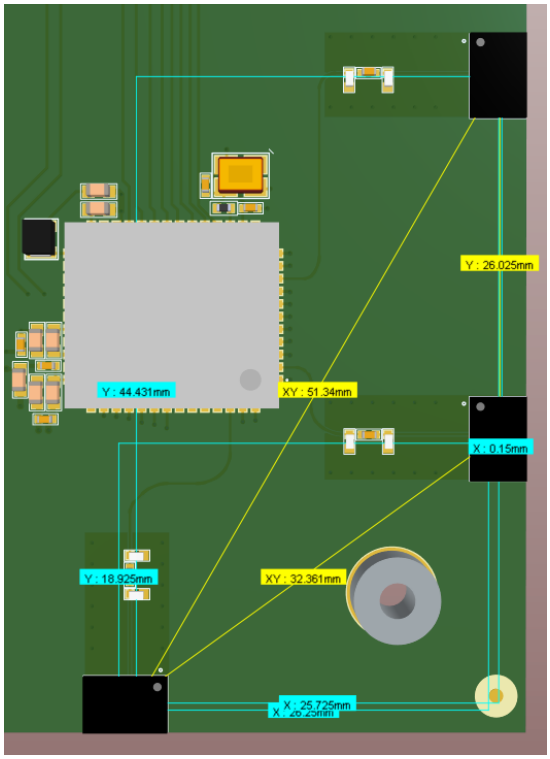


Fig. II.29 WIFI/BT antennas distances

8. Analog power layout

The system can be powered through 2 power paths. Both paths need to sustain the current values discussed in the power management chapter. The PMIC will be limited by hardware and software to 3A. The tracks should support this current and it is needed to take a safe margin of at least 10%. The power planes are routed on L3 and referenced to L2 which is a solid GND.

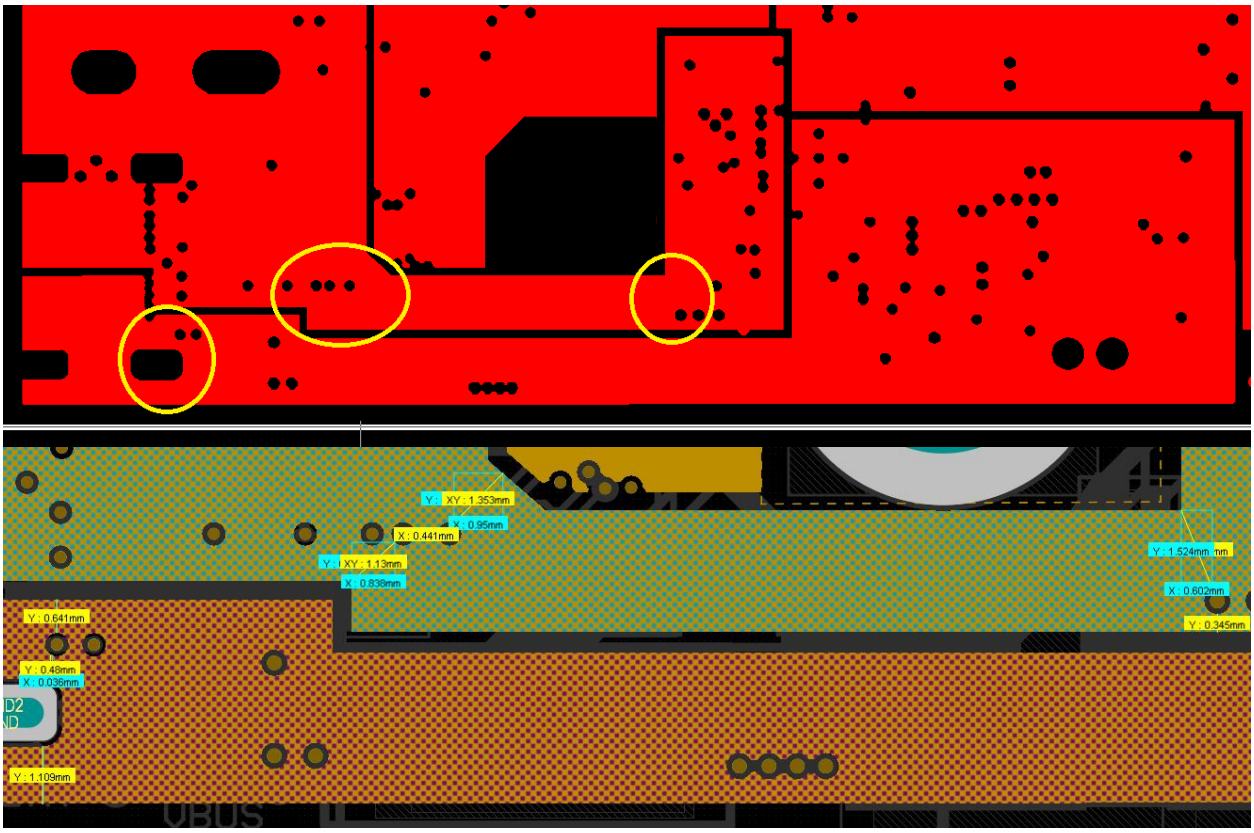


Fig. II.30 Concerning areas in the layout regarding the current flow

The questionable areas of the design are marked with yellow in figure 30. These areas are the smallest and will need to carry the highest amount of current on the PCB. Initially, these areas were even smaller, but after finding out that the current is too high, the design was improved to raise the limit that can flow through them. The current tracks can sustain at least 3.3A with an increase of temperature of 10°C.

Fig. II.31 Current supported by different track width (Saturn PCB Toolkit)

The power layout is confined in the corner of the board where on top layer is the Type-C connector and right beneath, on bottom layer, the battery spring connector. Both current paths have the same characteristics and are not conflicting with high speeds signals because are also shielded by GND planes to avoid the crosstalk. [13]

III. Results

The designed PCB was manufactured by an external assembly house and it took 2 weeks to be ready for a total cost of approximately 400 USD/pcs. The final layout is shown in figure 1. Providing power though USB Type-C connector the system boots up the Android OS from the first try, which is by itself a great success.

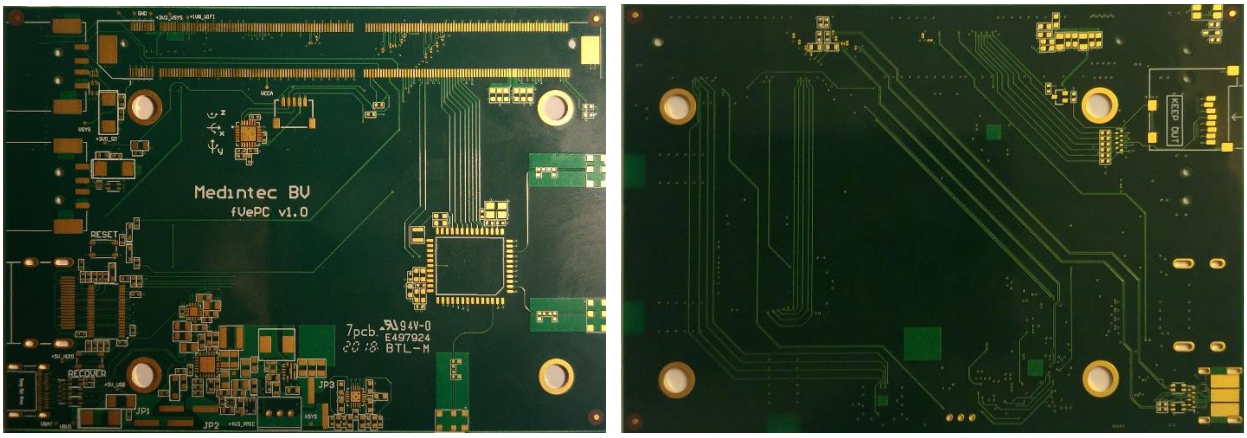


Fig. III.1 Top and Bottom manufactured PCB without components

After the boot up, all interfaces were tested. The HDMI port is working properly being connected to a monitor, the mouse works through USB 2.0, SD card is read by the interface, gyroscope works, and the WIFI/BT connects to the network. All features were tested and are fully functional within the requested parameters.

The application that will run on this device consists in VR content which ran smoothly for the entire period. The temperature sensors from CPU and GPU indicate 50°C in idle state and rise to 65-70°C in full load. The battery temperature range is between 28 to 36°C, varying with the increasing current which is influenced by the decreasing voltage of the battery. Fully charged battery has 4.2 V and lowers to 2.8V near full depletion. The temperature was tested with NTC included inside the battery pack.

1. USB 2.0 eye diagram

In figure 2 is presented the eye diagram for the USB interface when communicating with the mouse. The frequency is 12 MHz being the standard for USB 2.0 normal speed, which is enough for a mouse. The eye diagram is a qualitative representation of the signal integrity. The eye is composed from the bit transition and in the ideal case it looks like a rectangle. To display this kind of diagram the oscilloscope persistency value needs to be set high or infinity and the trigger should be made on an external clock or a recovered clock from the data signal encoding. In reality, the transitions are not perfect, thus noise and jitter appear and create an eyed shape diagram [14]. The USB 2.0 diagram presented can be analyzed and several facts can be extracted from it:

- Zero and one levels are the mean values of the signal logic levels. The results show a constant, clean logic levels without ringing.
- The eye height measures the eye opening and in the ideal case should be equal with the signal amplitude. It provides a good understanding from the noise point of view. It can be observed that the analyzed signal has a portion that is affected by noise, being a little closed in the left side of the bit width. Overall the SNR has a decent value that does not impact the functionality.
- Eye crossing percentage is a factor that shows if the duty cycle is 50% as it should be for a digital signal. The level where the crossing level is placed determine the percentage of eye crossing by expression: Eye Crossing % = 100 * [(crossing level – zero level)/ (one level – zero level)]. In this case, this percentage is between 50-52% which is a good indicator that the signal has a good pulse symmetry and no distortions.
- Jitter is the ability of the signal to not deviate from the ideal timing of data-bit. It is one of the most important characteristics when a high speed digital signal is analyzed with the eye diagram. It can be observed that in the signals presented, the jitter is approximately 5ns, which is a proper value for an 83ns signal period.

Overall, the USB 2.0 interface has a good performance and this is concluded from the eye diagram.

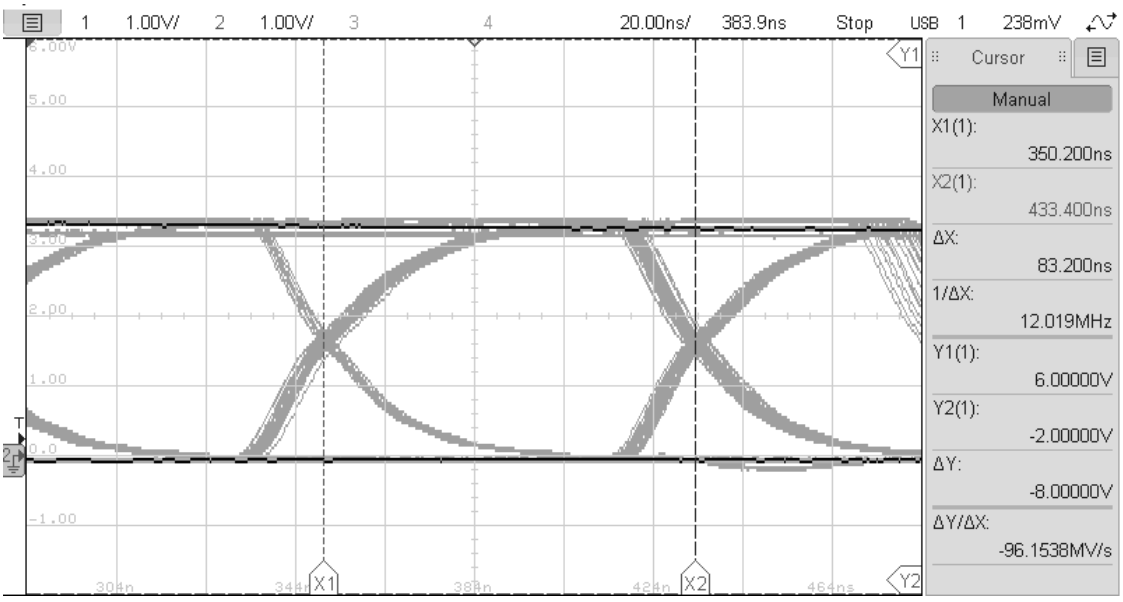


Fig. III.2 Eye diagram of USB 2.0 interface (tested near the connector)

2. WIFI signal strength

WIFI signal was tested using an application (WIFI Analyzer) installed on Android. The testing procedure involved placing the system at certain points from the access point to assess the quality of the signal in relation to the distance.

Figure 3 shows that the best signal strength is at maximum 1m from the source and decays with approximate 10 dBm/m which is a high degradation rate. This implies that the performance of the WIFI antennas is low and this can be due to the poor tuning of the matching circuit for the specific system characteristics. Other plots shown in the figure are the other WIFI networks presented in the moment of testing in the same area with the connected AP. They have no meaning for the current test and it can be considered noise. The application just does not have the ability to hide them. Internet connection speed is normal in the short range of the AP, but it is a problem when it gets further away from it. This is a subject that needs improvement in the next revision of the product.

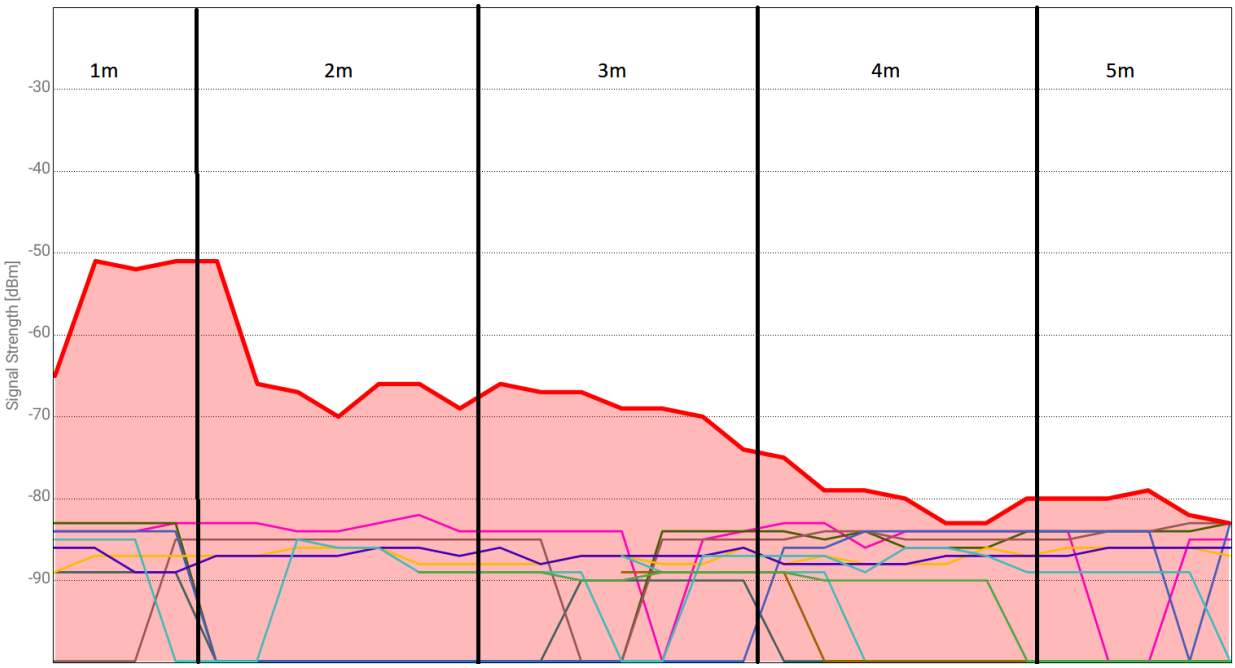


Fig. III.3 WIFI strength signal at different distances from the access point

3. Battery life-time

The battery chosen is a single cell rated as 6000mAh capacity @ 3.7 V. To ensure that these ratings are correct a battery test was performed where the current, voltage and temperature were observed from full capacity of the battery until depletion. The simulated power consumption was 12 W with 0.5 W loss.

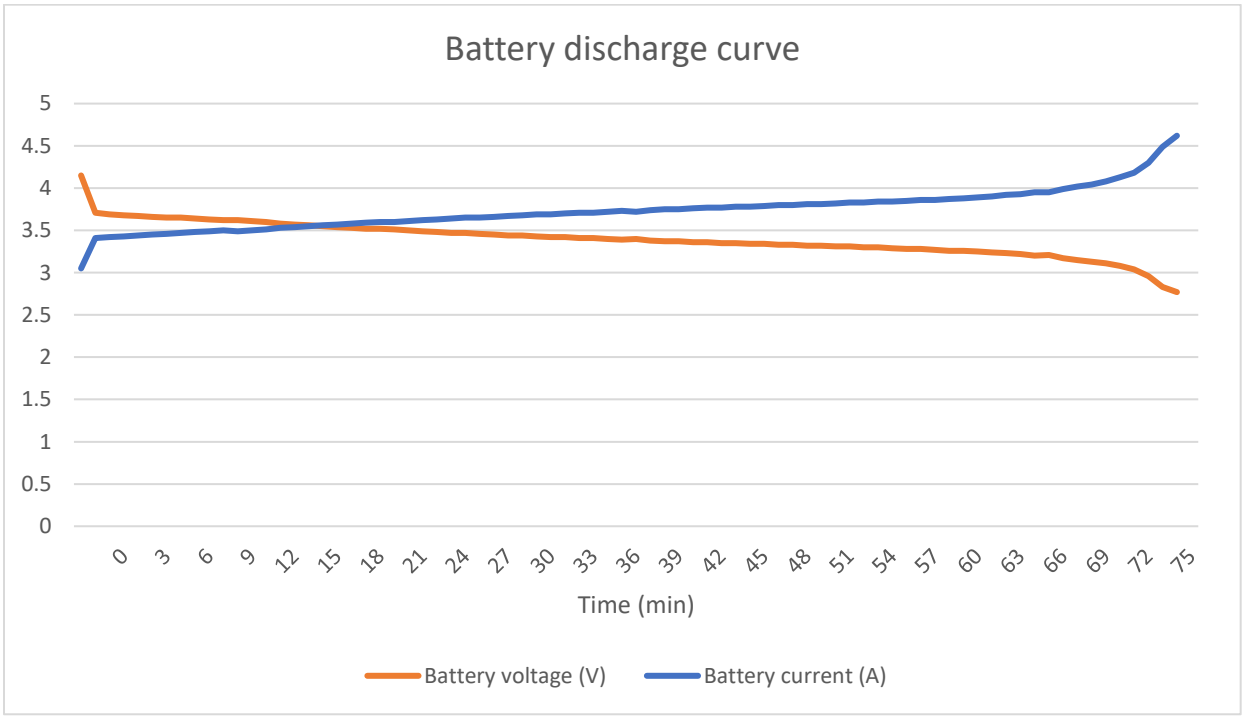


Fig. III.4 Battery discharge curve

It can be observed in the figure that the battery effective rating is not the real one. The calculated battery life for this application in Chapter 3.1 was enough for 1.5 hours of runtime. The current battery is rated at 6000mAh, but in reality, the effective capacity is around 4200mAh. If the calculus is changed with this new value of capacity it will show that indeed the runtime decrease around 1 hour. So, the battery needs to be replaced with one with a higher capacity or with a higher effective capacity. This difference between rated capacity and actual capacity can be explained due to the safe regulations induced by the manufacturer. In the figure of the temperature, it can be observed that the longer the battery lasts, the higher the temperature gets due to the increase of the current drawn by the application. This increase is produced by the need of the boost converter to sustain the same power amount through the decreasing VBAT. By increasing the drawn current to charge the inductor, the boost converter is able to sustain the system main power rail voltage.

The battery temperature safe range stops after 1 hour of runtime. After this, the temperature raises over 40°C and can damage itself or it can affect the user experience, heating all the system excessively.

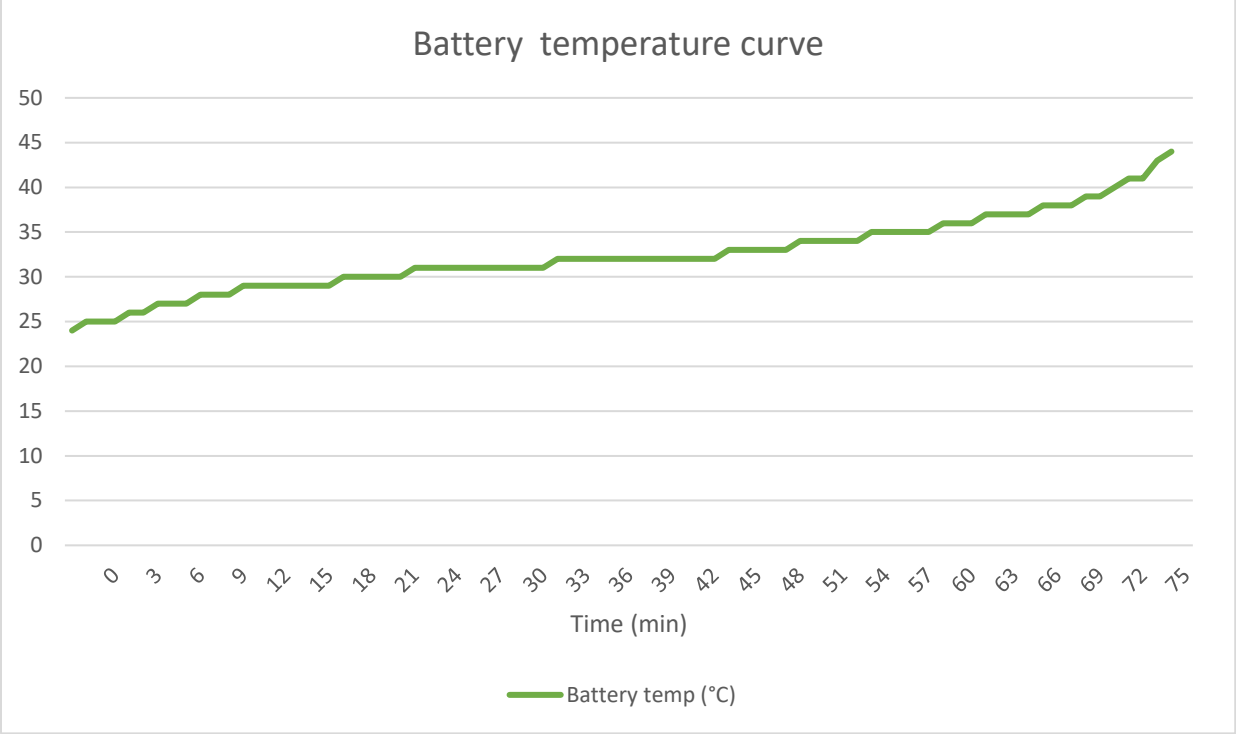


Fig. III.5 Battery temperature curve

IV. Conclusion

I designed a fully functional carrier board for a SOM that will be used in VR HMDs applications. The main requirements of the project were clearly stated by the stockholders of the project and the most important ones were the **cost, form-factor, performance and reliability**. All design choices were made by keeping all this in mind.

High-speed digital interfaces design is facing many challenges from the EMC point of view. There are many differential pairs involved which need greater attention to be matched properly for their impedance requirements and also to avoid mixing them up with other types of signals in the system. Routing this kind of signals is the top priority and I thought about it in every project phase since the beginning of component placement. From the analyzed results I can say that the development is within the required standards and the interfaces are working as expected.

Analog power management challenge is about ensuring a good isolation and providing a clear strong path for the high current that will flow through system. The temperature and energy leakage from these tracks are a real concern and had to be addressed as well from the first stages of the development. That is why this part was confined in a corner where the power connectors are located, to limit the thermal and noise issues.

RF module (WIFI/ BT) is the domain that I had the least experience in and where the antenna tuning is a really hard task because it ca not accurately be estimated through calculus and a practical approach will always provide a better result. As shown in the Results chapter this module needs to be improved in the further revisions because the performance achieved does not match the rest of the system.

The complexity of this project relies on the **aggregation** of electronics fields involved such as high speed digital interfaces, analog power management and radio frequency module. The space available on the PCB makes the task even harder because of the different modules that should be separated to avoid interferences, crosstalk and in the end the malfunction of the entire product. Above this, the time allocated for design was short, as a normal development of this kind of project would take on average 6 months. Integrating all the modules, it creates a lot of chance that some errors can appear, but despite all of this the project was a real success.

The most interesting part in this project is the fact that after first prototype, this PCB can compete at a decent level with others VR goggles available on the market in terms of features, cost and in some cases also from performance perspective.

In the end, the most important aspect is that I designed a product that has a practical application and can be used in multiple ways by many users. The VR goggles are an important player on the technology market in this moment and by developing a device like this with **real life requirements** and with **real life problems** made the whole master program a lot more valuable for me.

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